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1759(A-2)

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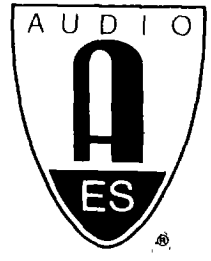
Presented at the 69th Convention 1981 May 12-15 Los Angeles



AN AUDIO ENGINEERING SOCIETY PREPRINT

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Abstract

Two LSIs and one IC have been developed for PCM digital signal processing based on a PCM standard format. These two LSIs and one IC can provide the same processing capabilities as about 500 conventional logic ICs, thus allowing much more compact dimensions for digital signal processing.

The LSI MN6601 is employed for recording the PCM digital signal :it takes the A/D (Analog-to-digital) converted digital data, adds the error detection code and correction code and outputs them as video data.

The LSI MN6602 is used during playback to reconstruct the PCM digital signal, carry out error correction and provide this as serial data to the D/A (digital-to-analog) converter.

The IC AN6860 is used for time-base generator and other accessory circuit for the A/D and D/A converters.

1. Introduction

In recent years a great deal of progress has been made in electronics technology and, particularly, in digital techniques and LSIs, and many new techniques have reached the stage of practical application through the adoption of the expertise evolved with this progress.
In the area of audio technology, recent trends have seen the rapid adoption of digital techniques, and these have had a great effect

on PCM recording/playback units produced by combining VTRs with digital techniques, in that their high-fidelity performance is far superior to that of conventional tape recorders.
What the authors have done is to configure the whole circuitry of the digital processing section, based on PCM standards, with two LSI chips and also successfully apply these chips for practical purposes.
One LSI (MN6601) is used for PCM encoding; the other LSI (MN6602) is used for PCM decoding. NMOS 4μ processing technology is adopted.
With both chips the maximum operating frequency is a high 17.5 MHz and the input/output pins feature a TTL compatible configuration.
Because of the differences among the television systems, VTRs come in two field frequency types: 60 field types (NTSC) and 50 field types (PAL, SECAM). There are PCM standards for each type and the above LSIs can be used with either type.
In addition, the authors have also developed an IC (AN6860)as a logic device for the analog-to-digital and digital-to-analog converter periphery. This adopts a high-density and high-speed IIL process and displays a propagation delay time of 25 nanoseconds/gate. These LSI chips and IC have made it possible to increase the accuracy, stability and reliability of the PCM digital signal processor.

2. LSI MN6601 for PCM Encoder

2-1. Features

The MN6601 LSI is for PCM encoding. The already A/D converted digital data are fed in and fed out as video data. It deals with dropouts in the data by adding an error detection code and error correction code and it performs data interleaving simultaneously. An external LSI memory is required for the interleaving operations and the addresses for this are also generated. This LSI may be used with a NTSC TV system or with the PAL and SECAM system, and the PCM standards are conformed to in each case.
Besides for a single-unit deck, it is also possible to use this model for a PCM adaptor, in which case the VTR's recording and playback mode are detected automatically. The configuration also contains functions to provide compatibility with peripheral units such as a control word writing function for editing applications and an address control function for simultaneous recording.
Furthermore, by combining this LSI with the MN6602 LSI used for PCM decoding, it is possible to carry out digital dubbing. All the PCM encoding operations are performed with this one LSI.

Sufficient consideration has also been given to the test functions of the LSI itself and all the functions of the LSI can be tested separately with test bit processing.
An outline of the MN6601 is given in Table 1.
Fig. 1 shows a photograph of the chip and the configuration of the functions on the chip.
Fig. 2 is a block diagram of the chip.
Fig. 3 shows the frequency relationship between the clocks in the NTSC TV signal format and Fig. 4 shows the same for the PAL and SECAM TV formats.
The following description is confined to the PCM signal processing based on the NTSC TV format, and details for similar operations in the PAL/SECAM TV format will be noted in the section on the PAL/SECAM version.
The PCM signal format is in accordance with the television standard, one filed (262.5 H) containing a data block of 245 H and a control signal block of 1 H.

2-2. Data Block Structure

One data block consists of six sampled signal words, P and Q error-correcting words and one error-detecting word (CRCC).

2-2-1. Signal Data Input Interface

The LSI MN6601 is capable of processing two sets of two's complement binary coded 14-bit serial digital signals.
One input is the A/D converted signal and the other is the digital dubbing input. In either case, sampling is done on channels A and B alternately in order to stagger the sampling time (Fig. 5).
One of the two systems in the LSI is selected and processing performed. Fig. 6 shows the data block input interface section and Fig. 7 shows the data configuration and timing.

2-2-2. The Processing of Error-Correcting Words

The error-correcting code is called the "interleaved matrix code" which can correct two error words in six words. Each of the error-correcting codes, P and Q, consists of 14 bits.
Fig. 8 shows the relationship between the six data words and the two error-correcting words, P and Q.
In the figure, data words W1, W2, W3, W4, W5 and W6 correspond to data words Ln, Rn, ..., Rn+2, respectively as indicated in Fig. 5.

Error-correcting words P and Q are generated according to formulae (2-1) and (2-2), as follows:

$$P = W1 \oplus W2 \oplus W3 \oplus W4 \oplus W5 \oplus W6 = \sum_{i=1}^{6} Wi \qquad (2\text{-}1)$$

$$Q = T^6W1 \oplus T^5W2 \oplus T^4W3 \oplus T^3W4 \oplus T^2W5 \oplus TW6 = \sum_{i=1}^{6} T^{7-i}Wi \qquad (2\text{-}2)$$

Note: $\oplus$=Modulo 2 summation of bits in each column.
In addition, "T" is the Q generating matrix which is shown below.

$$T = \begin{bmatrix} 0&0&0&0&0&0&0&0&0&0&0&0&0&1 \\ 1&0&0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&1&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&1&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&1&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&1&0&0&0&0&0&1 \\ 0&0&0&0&0&0&0&0&1&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&1&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&0&1&0 \end{bmatrix} \qquad (2\text{-}3)$$

2-2-3. Encoding of Error-Correcting Code

The way in which the error correcting code is generated in the MN6601 LSI is now described.
The P code is generated by forming an exclusive OR with every data bit, as in Fig. 9, and in the case of serial processing, configuration is made with a 14-bit shift register and on EOR gate.
The Q code is generated as follows.
The matrix "T" is the associated matrix of polynominal $X^{14} + X^8 + 1$, and the multiplication of matrix "T" is executed by the linear shift register, as shown in Fig. 10.
A shift by 1 in this circuit corresponds to the multiplication of the matrix "T" to the contents of the shift register.
In this circuit, the AND gate is first closed and W1 is fed in succession from MSB.
When the AND gate is opened by t_1 after the input operation and a shift is made by 1 in excess, TW1 remains in the shift register.

When W2 is fed in, W2 $\oplus$ TW1 remains in the shift register and when a shift is made by 1 in excess, the contents of the shift register become:

$$T\ (W2 \oplus TW1) = TW2 \oplus T^2W1 \qquad (2\text{-}4)$$

When input is fed in succession up to W6, the Q code is generated in the shift register.

2-2-4. Error-Detecting Word

The error-detecting word (CRCC), expressed as a 16-bit word, is the remainder which results from the fact that the sum of the six sampling words and one each for the P and Q words, giving a 112-bit signal in total, is divided by the following generating function:

$$G(x) = X^{16} + X^{12} + X^5 + 1 \qquad (2\text{-}5)$$

In this LSI the CRC code generating shift register employs an all "1" preset system whose configuration is shown in Fig. 11.

2-3. Data Block Assignment

2-3-1. Interleaving

In order to convert the burst-like dropouts formed on the VTR tape into random dropouts and to greatly improve the error correction capability, the P and Q error correction words and six sampling data words on the 1 H line have a 16 horizontal line interleaving distance (=D) and they are aligned on 1 H. Fig. 12 shows this arrangement.

2-3-2. Word Assignment

Each word after the interleaving is arranged in the order of six sampling words, the P and Q error-correcting words and error-detecting word generated from the formula given in section 2-2-4. Fig. 13 shows the resulting one data block.

2-3-3. Data Block Assignment Generator

The delay methods for obtaining the interleaved data words is the most essential part of the "interleaved matrix code" generator. As shown in Fig. 12, comparatively large memories are required for constructing the delay method.

In order to provide the above-mentioned delay, this LSI employs a random access memory (RAM) which is configured with four general 4 kilobit (4 bits x 1 k) memories.

* Memory Configuration

Fig. 14 shows the memory configuration for data interleaving. As is shown, the whole memory is considered as a single ring. This ring is apportioned into each of the interleaving lengths (D, 2D, 3D, ..., 7D) required for each data. The writing of the data is performed at the area marked WR(i) in the figure and readout is performed at the RE(i) area.
When the writing and readout for data amounting to a single block are completed, each of the writing and readout points is rotated clockwise by an amount equivalent to a single word. This clockwise rotation means that the memory address is advanced by an amount equivalent to one word.
As described above, every time the data of a single block (8 words) are written and read out, the writing and readout points are rotated clockwise by an amount equivalent to a single word to perform interleaving. There are no parts of the memory which are not used and so use can be made with 100% memory efficiency.
The writing address of the LSI for realizing the above memory configuration is now indicated.
If the values corresponding to two buffers and the interleaving distance corresponding to each word are added to each other when the words are written, the word addresses can be decided. In this way, the Wl address is advanced by an amount equivalent to one word when the writing of data in a block is completed.
By the above process the writing address can be sought [WR(i)].
If the readout address [RE(i)] is considered in the same way centering on Rl, then the RE(1), RE(2), ..., RE(8) addresses can be sought as +0, +α, +(2α + D), +(3α + 3D), ..., +(7α + 21D).
Fig. 15 shows the above configured circuit block.
When the memory is used, the memory address reset method must be considered. When the writing address and readout address coincide, the correct data cease to be read out since the data during writing are read out. This means that when these two addresses coincide, it is necessary to reset the address counter. In this particular LSI, the memory has the configuration as described above and so the zone between the writing address and readout address is detected for address resetting. This is shown in Fig. 16.

2-4. Control Signal Block

2-4-1. Word Assignment

The words are arranged as follows; cueing signal word, content-identification signal word, address signal word, control signal word and error-detecting word. The words are arranged in a single data block as shown in Fig. 17.

2-4-2. I/O for Control Signal Block

Any setting is possible for the total of 56 bits, after the 56-bit cueing signal, in the control signal block. This particular LSI contains a 56-bit buffer memory, and the external 56-bit input DATA is stored in this 56-bit memory and it is possible to arrange it at the 56-bit position in the control signal block.
Fig. 18 shows the I/O configuration of the part and timing.

2-5. PCM Signal Waveform

2-5-1. Assignment and Structure

Fig. 19 shows the data asignment and configuration within 1 H while Fig. 20 shows the assignment and configuration within 1 V.
Fig. 21 shows the signal waveform and level.

2-5-2. I/O for PCM Signal Waveform

This LSI contains a circuit that generates the data and timing values shown in Figs. 19 and 20.
Fig. 22 shows the above signals fed out from the LSI and their timing values.
Fig. 23 shows the actual I/O circuit.

2-6. Digital Dubbing

As was already mentioned in section 2-2-1, digital dubbing can be performed quite easily by adding the reproduced digital data to input port.
Fig. 24 shows the configuration for digital dubbing. The MN6602 LSI used here is for the reproduction of the PCM digital signal. Digital dubbing involves reproducing the recorded PCM digital signals and recording the PCM signals onto another VTR again. Since dropouts and other errors produced during the reproduction are corrected, there is absolutely no deterioration in the quality of the recording.

Required for digital dubbing are F_{ADCK} timing synchronization and left/right channel sampling synchronization between the playback and recording signals. As shown in Fig. 24, all the signal synchronization is made possible by the connections illustrated between the two LSIs.

2-7. Digital Audio System

Besides the PCM standard-based format functions, this LSI has many other functions which are required because of the configuration of the digital peripheral units.

2-7-1. Automatic Recording/Playback Identification Function

This LSI has a function which automatically identifies the recording and playback modes of VTR in consideration of cases where its use may be made as a PCM adaptor.
The modes are actually identified through coincidental detection of the CRC data during a 10 V period.
Fig. 25 is a block diagram.

2-7-2. Synchronized Recording System Function

By using "n" number of this LSI, it is possible to perform 2 x n channel PCM multi-channel recording.
A synchronizing signal generator and synchronizing signal receiver are available for this purpose and by presetting the address registers and timing counters inside the LSI, multi-channel recording is made possible.
Fig. 26 is a block diagram.
It goes without saying that the signals synchronized with the MN6602 are provided in each case.

2-7-3. Master/Slave Modes

This LSI is operational in both the master and slave modes. It is also possible to select the MN6601 serving as master or slave mode where operation is provided while the clock systems obtain synchronization with other master MN6601 LSI.
The master clock system, Ftrans system and F_{ADCK} system are the clock systems which are selected by the master/slave selection.

2-8. PAL/SECAM Version

Simply by means of 1-pin control, this LSI can be switched to conform to NTSC or PAL/SECAM TV system standards. With the PAL

and SECAM systems, the applicable PCM standards are those which are based on the 625-line TV format.
Fig. 27 shows the configuration using a PLL circuit which is designed to generate the F_{ADCK} clock pulse for the PAL/SECAM system.
There is a reason for using a PLL circuit: by giving the master clock oscillation frequency a value approaching that used for the NTSC system by means of PLL, uniformity has been produced in the operating frequency region, and the creation of the LSI has been facilitated.

3. MN6602 LSI for PCM Decoder

3-1. Features

The MN6602 LSI is designed for PCM decoding. The PCM digital signals recorded on the VTR tape are taken out as playback signal by means of VTR playback and supplied to the D/A converter in the form of a 14-bit series output by MN6602. Both bit synchronization and clock synchronization are performed with the decoding operation, data error detection and error correction operations are performed in order to counter any dropouts in the data, and data de-interleaving, playback signal muting and holding processing are also carried out by MN6602.
A memory address generator circuit of the external LSI memory is provided for de-interleaving and VTR jitter absorption.
This LSI has a RAM which functions as the error detection result memory. It is used both with the NTSC system and PAL/SECAM systems, and is based on PCM standards in each case.
Use may be made either for a single-unit deck or PCM adaptor, and there is a timing generator circuit for the D/A converter.
Functions designed for compatibility with peripheral units include a control word readout function and an address control function for synchronized playback. All the PCM decoding operations are performed by this one LSI.
Sufficient consideration has also been given to functions which test the LSI itself. In fact, all its functions can be tested separately by test bit processing, and checks even including the F/F gate units can be carried out from outside the LSI in packaged form.
An outline of the MN6602 LSI is given in Table 2.
Fig. 28 gives a photograph of the chip and shows the arrangement of the functions on the chip.
Fig. 29 is a block diagram.
The following description concerns the PCM signal processing based on the NTSC format. Details on the processing for the PAL/SECAM TV format can be found in the section on the PAL/SECAM version.

3-2. Synchronization for Reproduced Video Data

The PCM signals are obtained by recording signals onto a VTR tape and then playing them back. Therefore, breaks in the playback signal will result or clicking noise will be generated unless there is perfect synchronization between the VTR signals and the LSI.
Any data errors caused by fluctuations in the synchronization cannot be corrected by the error correction code. This fact can be explained as follows. When data are disturbed from the PCM standard format at the vertical synchronizing signal section, it is then necessary to recognize properly where the data begin again. (This is known as obtaining V synchronization.) This is why a 56-bit "cueing signal" is inserted into the 1 H period head section at the point where the data start again. However, if dropouts cause the cueing signal to be ignored and the following H signal to be mistaken for the cueing signal, the data obtained will be correct even if this point is recognized as the starting point of the data, and so it will not be possible to detect the synchronization error with the error detection code. Consequently, the sound reproduced will be heard with a signal equivalent to 1 H missing and this recognition can be judged after the playback of the 1 V signal.
However, at this point it is not possible to judge whether the cause is a cueing error or dropout, and if, for instance, the cause is judged to be a cueing error, there is no way in which the incorrect sound can be processed because it has already been reproduced. In order to eliminate any trouble in the playback sound by synchronization errors, this LSI features a variety of ways in which to maintain the synchronization.

3-2-1. Bit Synchronization

Bit synchronization is provided by picking up the data sections from among the video signals which have been played back and by supplying them to the MN6602 LSI. What happens is that a data picking up clock is shaped and the data are clocked at the center of the data. Even if jitter is contained in the playback data, this is tracked reliably in the LSI and clock reproduction is performed.

3-2-2. Data Block Synchronization

The H synchronization of a data block is performed from the data and synchronization sections among the video signals which have been played back, and synchronization of each data word is obtained. The data block synchronization methods are the above-

mentioned bit synchronization, sync. detection and data synchronizing signal detection. Provision is made so that the data block synchronization is performed reliably even if some type of detection is not performed by data dropouts.

3-2-3. V Synchronization

V synchronization is a particularly important form of synchronization. The LSI detects the V sync. equalizing pulse and also the cueing signal which is contained in the "1100" repeat pattern and ensures that the V synchronization is carried out reliably.

3-3. CRC Detector

3-3-1. CRC Detector Circuit

Fig. 30 shows the circuit that checks at the playback side the CRC code which was generated at the recording side.

3-3-2. CRC Detection Synchronization

Every time 14-bit data equivalent to a word are brought together, the playback data are continuously written into the LSI's external memory. Simultaneously, error inspection is performed and the results of this inspection must be written into the memory inside the LSI. As shown in Fig. 31, the results of the error detection are produced after the data have already been written into the memory.
The inspection results and data must be read out simultaneously, and it is then necessary to supply them to the error correction circuit which is the next step.
In order that the above operation be carried out, the writing address within LSI is advanced one block of the data writing address outside of LSI, as indicated in Fig. 32. For readout, the data and error detection results can be provided simultaneously by reading out the data in LSI's memory and the data in external memory together with the data readout address.

3-4. Decoding of Error Correcting Code

3-4-1. Error Correction Scheme

The error correction code has a structure in which 2-word check bits are added to the 6-word data, and it can be used to correct

any 2-word errors. The P code is composed as illustrated in the formula below.

$$P = \overline{\sum_{i=1}^{6}} Wi \qquad (3\text{-}1)$$

$\overline{\sum}$ indicates modulo 2 summation.

Any 1-word error can be corrected using this P code. Let us assume that W2 receives the error to become $\hat{W2}$.

$$\hat{W2} = W_2 \oplus e \qquad (3\text{-}2)$$

"e" is the error pattern.

Since, with formula (3-1):

$$P \oplus W1 \oplus W2 \oplus W3 \oplus W4 \oplus W5 \oplus W6 = 0 \qquad (3\text{-}3)$$

then it is easy to understand that:

$$P \oplus \overline{\sum_{i=1}^{6}} Wi \oplus e = e \qquad (3\text{-}4)$$

Therefore, "e" can be calculated by modulo 2 summation of the P code and all the data words. From formula (3-2), the correct data can be restored from:

$$W2 = \hat{W2} \oplus e \qquad (3\text{-}5)$$

It is clear that the above can be established for any data, and even when ith data has received an error:

$$\hat{Wi} = Wi \oplus ei \qquad (3\text{-}6)$$

$$P \oplus \overline{\sum_{K=1}^{6}} Wk \oplus ei = ei \qquad (3\text{-}7)$$

$$\text{And so, } Wi = \hat{Wi} \oplus ei \qquad (3\text{-}8)$$

is used to correct the error.
When two errors have been formed or, in other words, when the ith and jth data have received errors,

$$P \oplus \overline{\sum_{K=1}^{6}} \hat{W_k} = ei \oplus ej \qquad (3\text{-}9)$$

Now, if

$$P \oplus \sum_{K=1}^{6} \hat{W}_k = S_1 \tag{3-10}$$

$$\text{then } S1 = ei \oplus ej \tag{3-11}$$

The Q code is expressed as below:

$$Q = \sum_{i=1}^{6} T^{7-i} Wi \tag{3-12}$$

Therefore,

$$Q \oplus \sum_{K=1}^{6} T^{7-k} \hat{W}k = S2 \neq 0 \tag{3-13}$$

When, therefore, the ith and jth data have received errors indicated respectively by ei and ej: (3-14)
S2 is indicated in the following formula:

$$S2 = T^{7-i}ei \oplus T^{7-j}ej \tag{3-15}$$

If both sides are now multiplied by T^{i-7}, then by replacement with:

$$T^{i-7}S2 = ei \oplus T^{i-j}ej \tag{3-16}$$

Then because of formulae (3-11) and (3-16):

$$ej = (I \oplus T^{i-j})^{-1} (S1 \oplus T^{i-7}S2) \tag{3-17}$$

$$ei = S1 \oplus ej \tag{3-18}$$

"I" is the unit matrix and each of the respective error patterns can be computed.
The condition here is that even with any i and j combinations, formulae (3-15) and (3-11) should be linearly independent.
If ei and ej are now sought, the original correct values can be sought through an exclusive OR relationship between the error code and ei/ej by means of the following formulae:

$$Wi = \hat{Wi} \oplus ei \tag{3-19}$$

$$Wj = \hat{Wj} \oplus ej \tag{3-20}$$

This completes the description of the error correction principle.

3-4-2. Error Correcting

A description is now given of the hardware used for the error correction performed by this LSI.
If j is made greater than i in formulae (3-17) and (3-18) which indicate the error correction, if the formulae are re-written as $K = j-i$ and if MK is made $(I \oplus T^{-K})^{-1}$, then formula (3-17) becomes:

$$ej = MK\ (S1 \oplus T^{i-7}S2) \tag{3-21}$$

Since i takes values from 1 through 5 and j from 2 through 6, K takes values from 1 through 5. Therefore, there are five kinds of MK matrices, M1 through M5. The MK matrices are stored in a ROM for the execution of the error correction and a sequential operation method was adopted.
With the operation of $Ti-7$, i-7 is a negative value and so T^{-7} may be operated first.
Through operation as described above, the reverse matrix of matrix T is prevented from becoming a variable and the hardware composition is simplified.
Fig. 33 shows the MK ROM.
Fig. 34 is a block diagram of the error correction circuit.
In Fig. 34 the calculation of syndromes S1 and S2 is performed by the same method as that at the generating side.
Since W1 through W6 and the P code are fed into the P register with modulo 2 summation, syndrome S1 is provided as a result and by feeding the T^{-7} processed W1 through W6 and Q code into the Q register, $T^{-7}S2$ is provided as a result. In the control circuit, the CRC result of H to which each of the data belong is checked and i and k (=j-i) are fed out.

After $T^{-7}S2$ has been computed, the Q register rotates without hindrance for i times in accordance with the value i which has been fed out from the control circuit. In other words, the syndrome calculation is performed i times without an input. With every calculation, matrix T is multiplied and so, as a result, $TiT^{-7}S2 = T^{i-7}S2$ is obtained in the Q register.

The S1 in the P resister and $T^{i-7}S2$ provided in this way are modulo 2 summed, MK is multiplied by the correction matrix circuit, a single error pattern ej is produced and this is fed out. In addition, ej and syndrome S1 are modulo 2 summed and fed out as the other error pattern ei.
Therefore:

$$ej = MK\ (S1 \oplus T^{i-7}S2) \tag{3-22}$$

$$ei = S1 \oplus ej \tag{3-23}$$

are calculated and each error pattern is computed. As shown in Fig. 35 in which the correction matrix operation appears, matrix MK is multiplied in line units.
With which matrix, M1 through M5, the operation is to be performed is determined by the difference K (=j-i) in locations of the two errors. In the figure, the k1, k2 and k3 3-bit signal is used to pass this value to the ROM. The value of a single MK matrix line is fed out as the R1 through R14 14-bit signal, the input bits (S1 $\oplus$ T^{i-7}S2) are given an AND relationship with data R1 through R14 equivalent to one line of the MK matrix and by modulo 2 summation, 1 bit of the error pattern ej is fed out. Therefore, 14 clock times are required for this operation.

3-4-3. Cases of Single Errors

The following three instances of single word errors can be considered and in each case the correction method is described below in order.

(a) $\hat{W}i$ only error

In this case, the error may be corrected using S1 or S2 although with this LSI, S1 is used for the correction.

$$ei = S1 \quad \text{or} \quad ei = T^{i-7}\,S2 \tag{3-24}$$

(b) $\hat{W}i$ and $\hat{P}$ errors

S1 cannot be used in this instance and

$$ei = T^{i-7}S2 \tag{3-25}$$

may be transformed as follows:

$$ei = I\,(T^{i-7}S2 \oplus S1) \oplus S1 \tag{3-26}$$

In this case, therefore, unit matrix I is selected as MK. This unit matrix is in the ROM in the form of Mo, just as with M1 through M5.

(c) $\hat{W}i$ and $\hat{Q}$ errors

The method described under (a) is used in this case.
If the error counter mentioned in section 3-4-2 is checked it is immediately identifiable as to whether the error is single or not. The P and Q errors are detected separately.

3-4-4. Data Hold and Data Muting

The previous value of the data are held when there are three or more error words. This LSI (MN6602) uses error correction codes to correct errors caused by dropouts but when the number of dropouts increases in the extreme, the errors can no longer be corrected. This is why a muting operation is performed in the LSI. The dropout generation rate is employed to detect the ON and OFF modes of the muting. In actual fact, the number of errors generated in a 1 V period is counted. The counter is provided with hysteresis for a stable and yet reliable muting operation.
The LSI is provided with a function that accepts or rejects the muting operation and it is possible to inhibit this operation when it will have any adverse effects even though there may be a high number of erros.

3-5. Memory Configuration

The external LSI memory has a capacity of 32 kilobits, and by providing a memory of 2 kilobits for each data, it serves to absorb the jitter generated by the VTR.
Originally, there was no really fundamental need to have such a large-capacity memory but jitter is produced by the VTR when this LSI is used as a PCM processor and the memory is designed to absorb it.

3-6. Control Signal Block

3-6-1. Emphasis Control

The single emphasis signal bit in the control signal block is detected and the de-emphasis control signal is provided to analog signal during playback.

3-6-2. I/O for Control Signal Block

The LSI has a buffer memory for the total of 56 bits after the 56-bit cueing signal in the control signal block and it is possible to read out the contents of the memory at any time. This means that it is possible to identify the contents such as absolute addresses on the recording tape and that it can be used for peripheral units. Fig. 36 shows the I/O configuration of this part and the timing.

3-7. Digital Audio System

Besides the playback function conforming to the standard PCM format, this LSI has other functions required because of the configuration of the digital peripheral units.

3-7-1. Synchronized Playback System Function

By using N number of the LSIs, 2 x N channel PCM multi-channel playback is possible.
A synchronization signal generator and synchronization signal receiver are therefore provided and by properly presetting the address counter and timing counter inside the LSI, multi-channel playback can be performed.
Fig. 37 is a block diagram.
Naturally, the synchronization signal is perfectly synchronized with the MN6601.

3-7-2. Timing for Digital-to-Analog Converter

This LSI generates the timing pulses for the D/A converter. The timing is shown in Fig. 38.

3-8. PAL/SECAM Version

Through 1-pin control, the LSI can select between the NTSC and PAL/SECAM TV systems. When PAL/SECAM has been selected, playback is based on the PCM standards which are in turn based on the 625-line TV format.

4. I^2L IC AN6860 for A/D, D/A Time-Base Generator

4-1. Features

The authors developed a new IC using the master slice method for control of the data converters centering on A/D and D/A conversion and for interconnection between these converters and the digital signal processing circuitry.
There were solid reasons why the master slice method was used for this IC (AN6860). A flexible design was considered so that the IC could be used not only for control of the A/D and D/A converters used in this system and for the transfer of the signals with the signal processing LSI but also for various digital audio units which will be developed in the future. As is generally known, ICs developed with the master slice method are already prepared with the basic circuit configuration for virtually all

the active parts and, mainly through aluminum pattern design for interconnection, it is easy to develop a special-purpose IC with a range of various functions.
An outline of this master slice IC now follows.

1) High-speed, high-density I^2L process used
Because of its high-speed operation, the propagation delay time per unit gate is about 25 nanoseconds (with a 100 μA injector current), and the IC is composed so that an integration of about 1,000 gates can be realized inside this one chip.

2) High-speed input/output circuits used
A high-speed buffer circuit using a Schottky clamp circuit is employed in order to configure input/output circuitry featuring good balance with the high-speed operation of the I^2L section. This part has been configured so that, by changing over the aluminum wires, it is possible to realize an input buffer and three kinds of output buffer (tristate, totempole and open collector).

3) Double-layer aluminum high-density wiring
Double-layer aluminum wires are used in order to house the 1,092 gate circuits and 25 input/output circuits efficiently and in order to provide high-speed operation with short wire lengths. These wires make it possible to reduce greatly the wiring area.

4-2. Circuit Configuration

This IC serves to control the A/D and D/A converters and also to transfer the signals between the special-purpose digital signal processing LSIs (MN6601 and MN6602) and the data converters. Fig. 39 is a block diagram of the AN6860 and an outline of the IC's specifications is given in Table 3.

5. Performance of Digital Signal Processing Block

Fig. 40 shows the composition of the digital signal processing block that uses the MN6601 and MN6602 LSI and the AN6860 I^2L logic IC.

6. Conclusion

Through the development of these LSIs and I^2L logic IC, it has now become possible to configure equipment, which in the past has used a vast quantity of general-purpose TTL ICs, extremely compactly and also to greatly improve the performance of the equipment.
A great deal of the success in this project may be attributed to the progress made recently in the semiconductor industry.
In the months ahead the authors are firmly committed to making full use of the many functions for peripheral equipment containing LSIs in the perfection of digital audio systems.

Acknowledgements

The Authors would like to thank sincerely to Mr. Masui, director, Mr. Obata, Manager, Mr. Hirose, Mr. Odaki of Stereo Division, and Mr. Nakajima, Manager, Mr. Kobayashi, Manager, Mr. Kosaka of The Wireless Research Laboratory, and Mr. Mizuno, director, Mr. Arita, Manager, Mr. Nishijima of Matsushita Electronics Corporation.

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1) Electronics Industries Association of JAPAN : "Technical File of Stereo Technical Committee, Video Technical Committee, STC-007 CONSUMER USE PCM ENCODER-DECODER

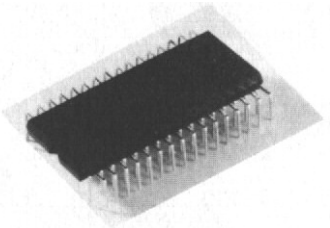
2) M. Kosaka : "Sampling-Frequency Considerations" Journal of the AES, p.p. 234-240 April 1978

3) T. Seno, et al. : "A Consideration of the Error Correcting Codes for PCM Recording System" the 61st AES Convention, preprint No. 1397 (H-4) November 1978

4) M. Kosaka, et al. : "A Digital Audio System Based On A PCM Standard Format" the 64th AES Convention, preprint No. 1520 (G-4) November 1979

Table 1. Basic specifications of LSI MN6601

	MN6601
Process	NMOS 4μ
Chip size	6.08mm x 5.58mm
Transister	About 10,000 Transister
Supply Voltage	+5 V
Operating Maximum Frequency	17.5 MHZ
I/O Inter face	TTL Compatible
Package	QIL 64 PIN



(a) MN6601

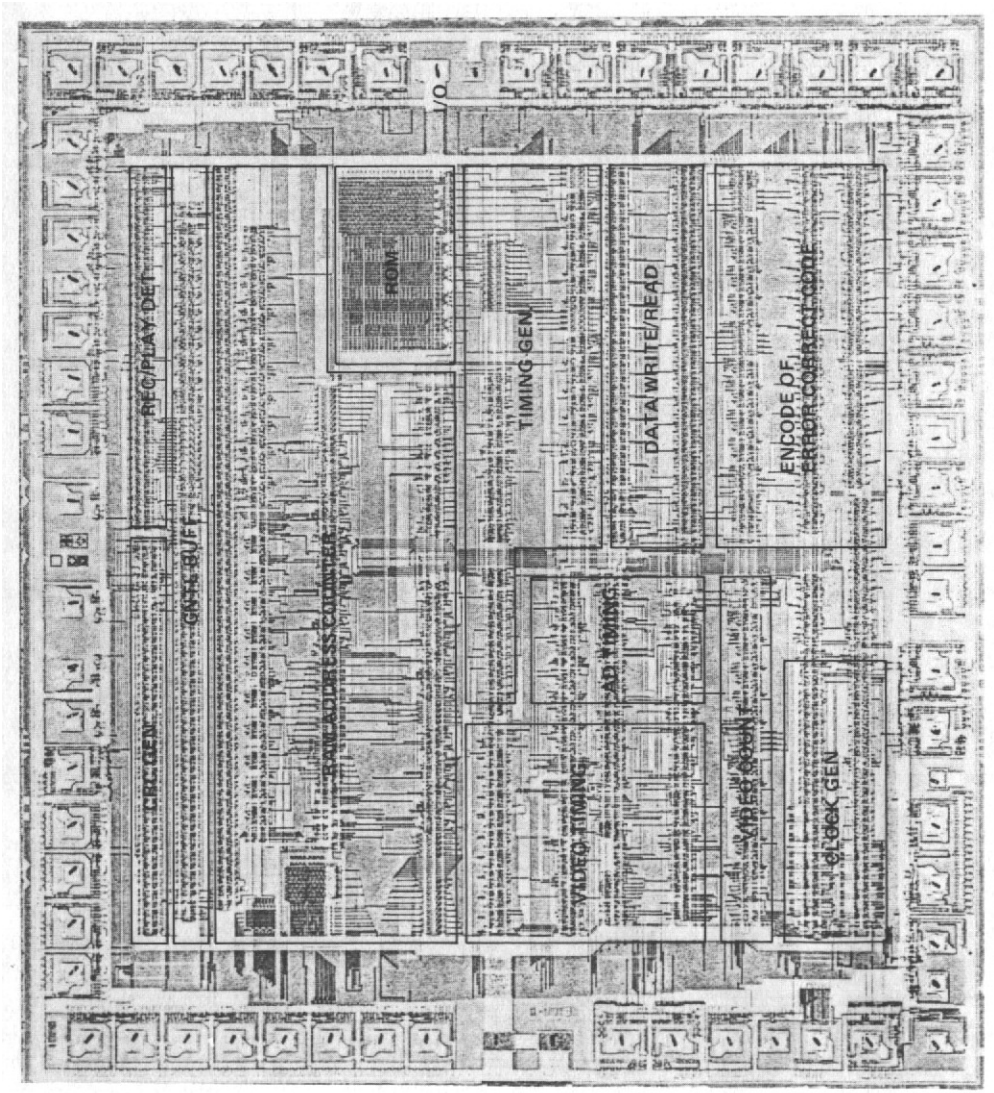


Fig 1 MN6601 CHIP

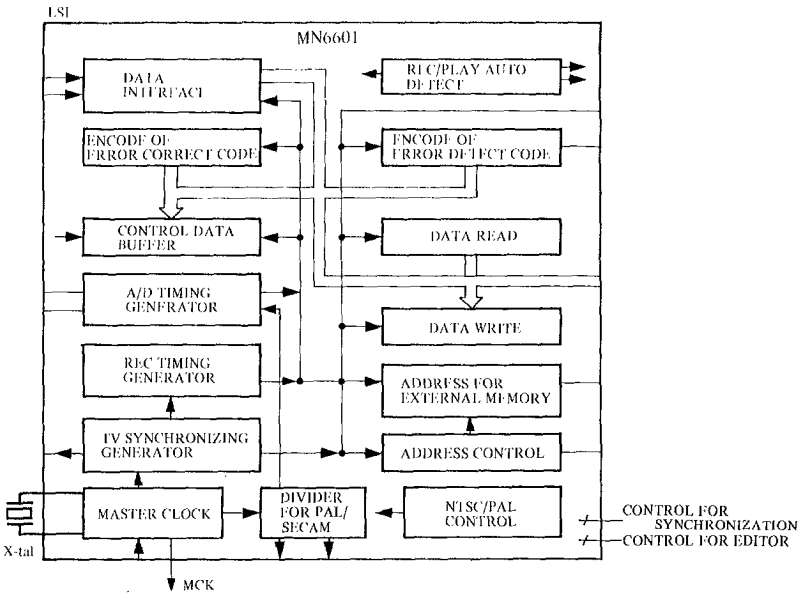


Fig. 2. Block Diagram of MN6601

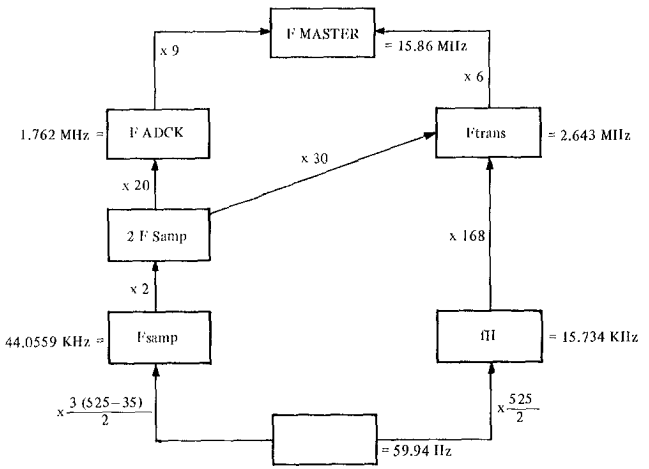


Fig. 3. Frequency relationship between FMaster and FV of NTSC

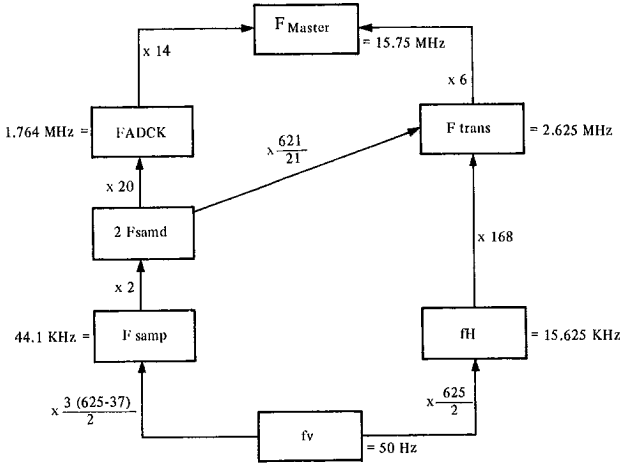


Fig. 4. Frequency relationship between F_{Master} and Fv of PAL/SECAM

Saupling time	2 N/2 T	2 n + 1/2 T	2n + 2/2T	2 n + 3/2T
L ch	Ln		L n + 1	
R ch		Rn		R n + 1
T = 1/ 44056 (sec)				

Fig 5. Sampling time

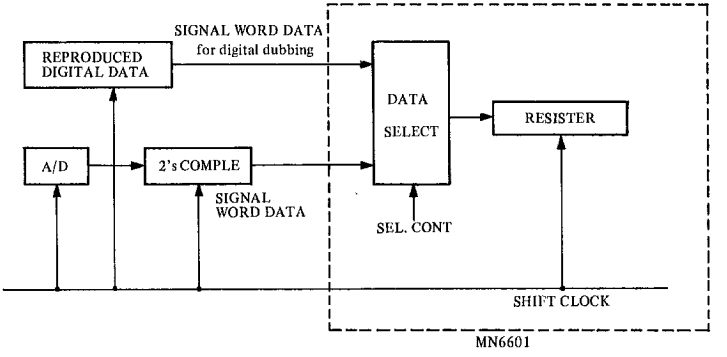


Fig. 6. Signal data input interface

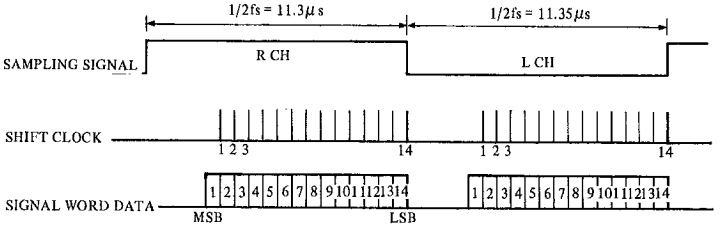


Fig. 7. Signal data structure and timing

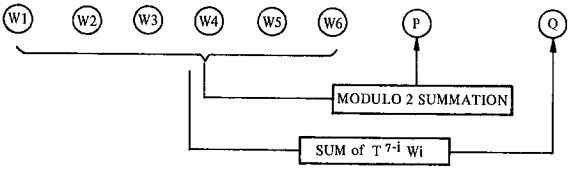


Fig. 8. Data words and error correcting words P, Q

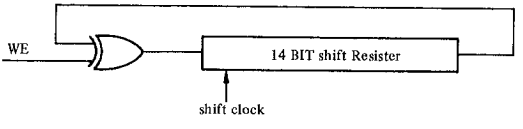


Fig. 9. P code processing circuit

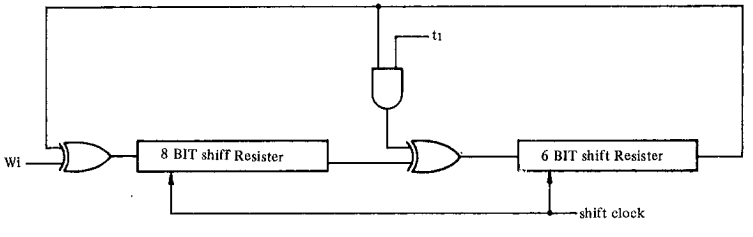


Fig. 10. Q code processing circuit

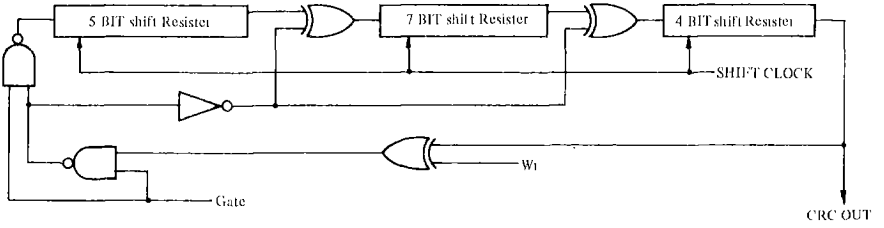
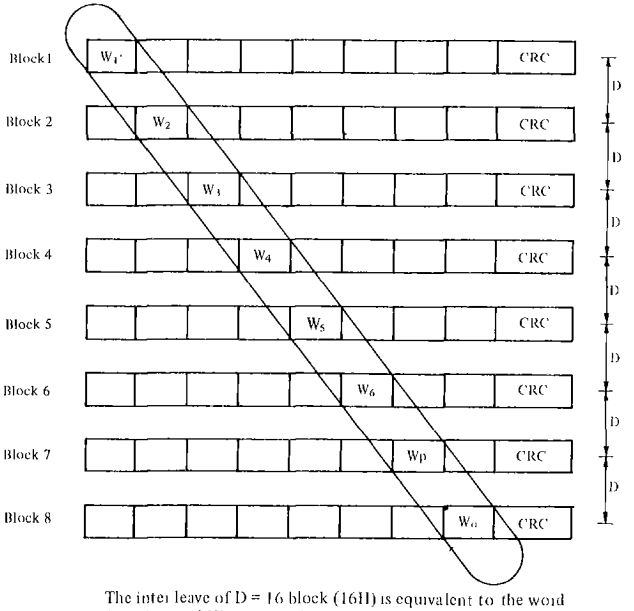


Fig. 11. Processing of CRCC



The inter leave of D = 16 block (16H) is equivalent to the word inter leave of 3D = 48 word.

Fig. 12. Inter leaved data allocation IN 1H

Ln	Rn-3D	Ln+1 – 6D	Rn+1 – 9D	Ln+2 12D	Rn+2 – 15D	Pn - 18D	Qn – 21D	CRCC

Fig. 13. One data block

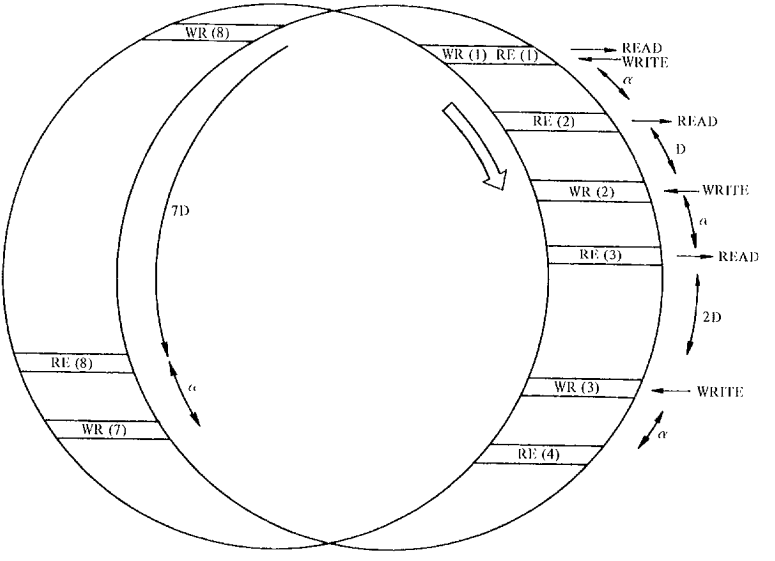


Fig. 14. Ring memory construction

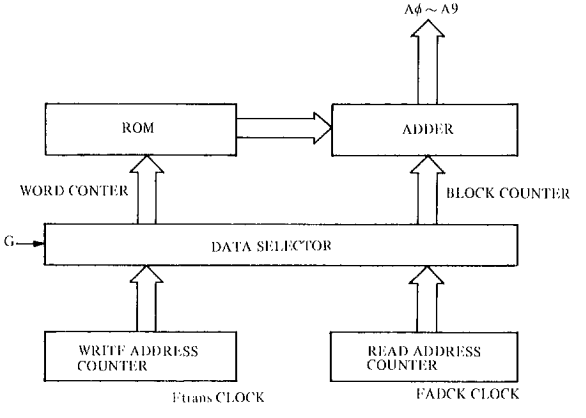


Fig. 15. Memory address

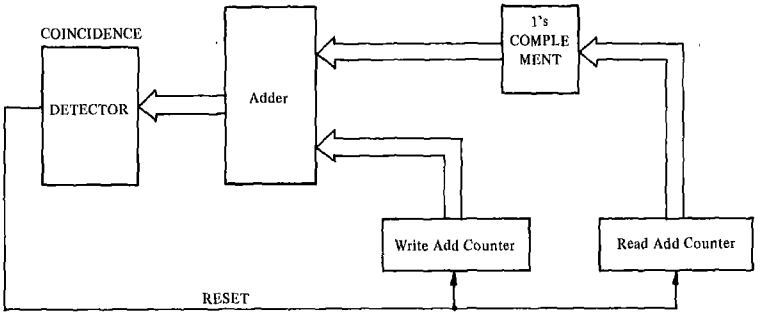


Fig. 16. Address reset

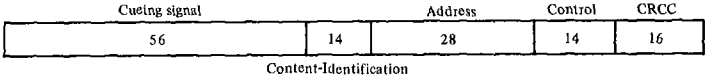
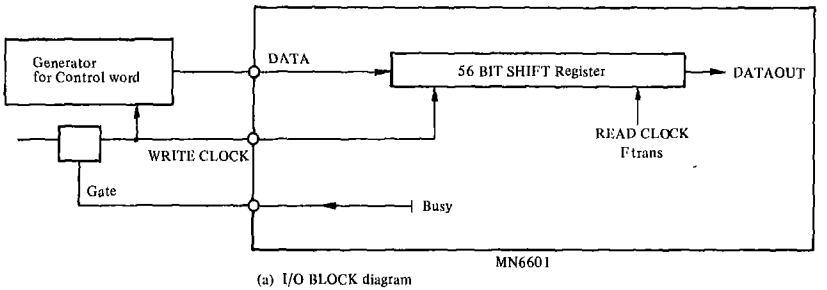
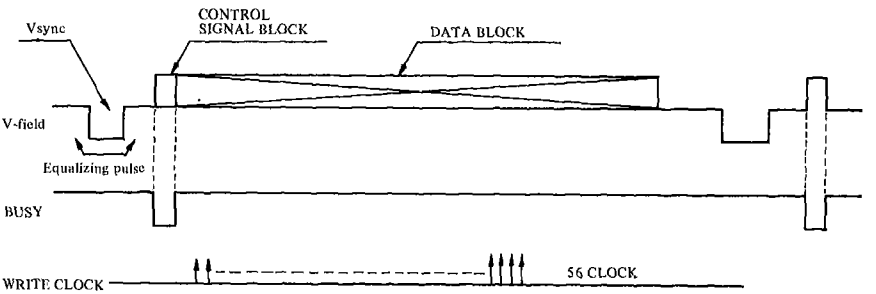


Fig. 17. Word assignment for control signal block



(a) I/O BLOCK diagram



(b) Timing for I/O

Fig. 18. I/O for control signal block.

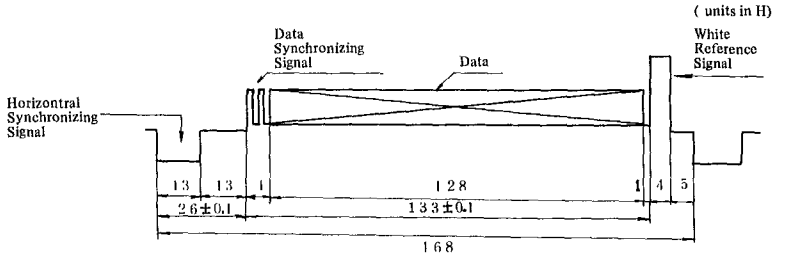
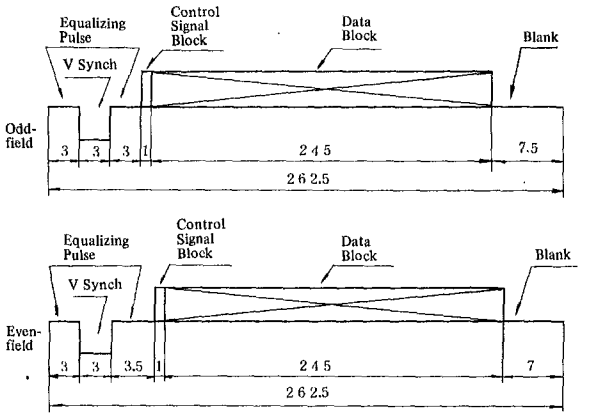


Fig. 19. Assign ment and strueture within 1H



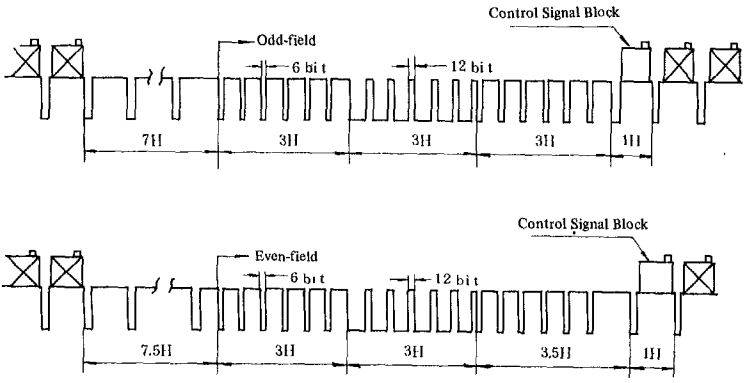


Fig. 20. Assignment and structure within 1V

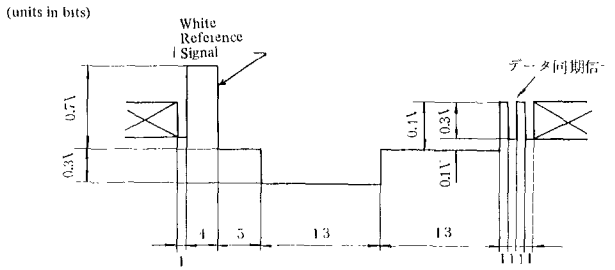


Fig. 21. Signal waveform and levels

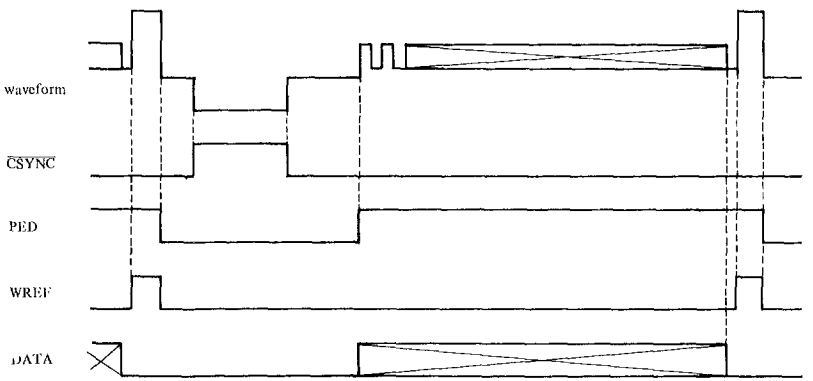


Fig. 22. Timing for signal waveform

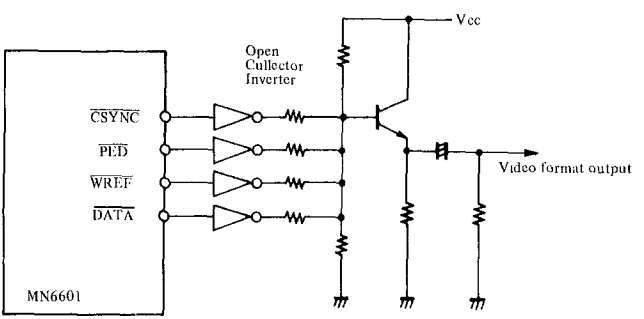


Fig. 23. Interface for video signal format.

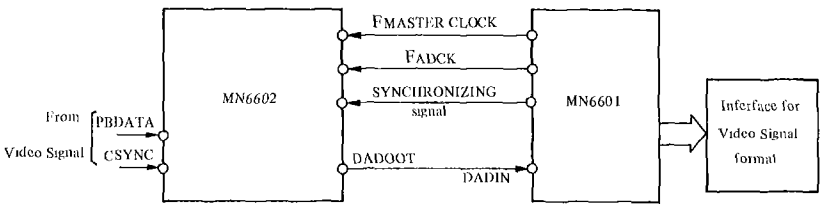


Fig. 24. Digital dubbing system

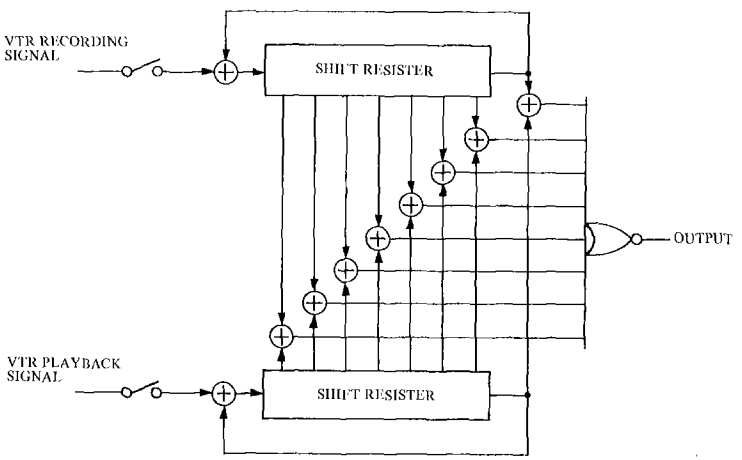


Fig 25 AUTOMATIC RECORDING/PLAYBACK IDENTIFICATION FUNCTION

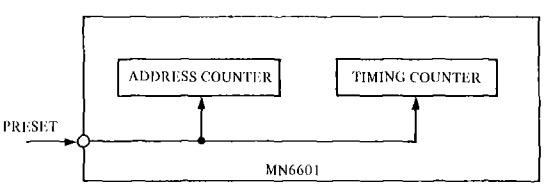


Fig 26 PRESET FOR SYNCHRONIZING

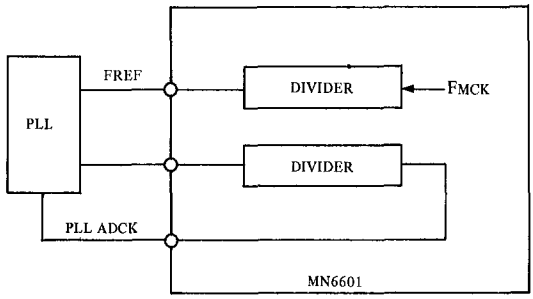
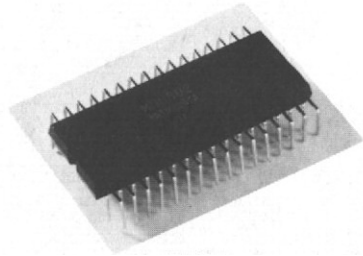


Fig 27 FADCK FOR PAL/SECAM

Table 2. Basic specifications of LSI MN6602

	MN6601
Process	MNOS μ
Chip size	6.46 x 6.18mm
Transister	About 15,000 Transister
Supply Voltage	+5V
Operating Maximum Frequency	17.5 MHZ
I/O Inter face	TTL Compatible
Package	QIL 64 PIN



(a) MN6602

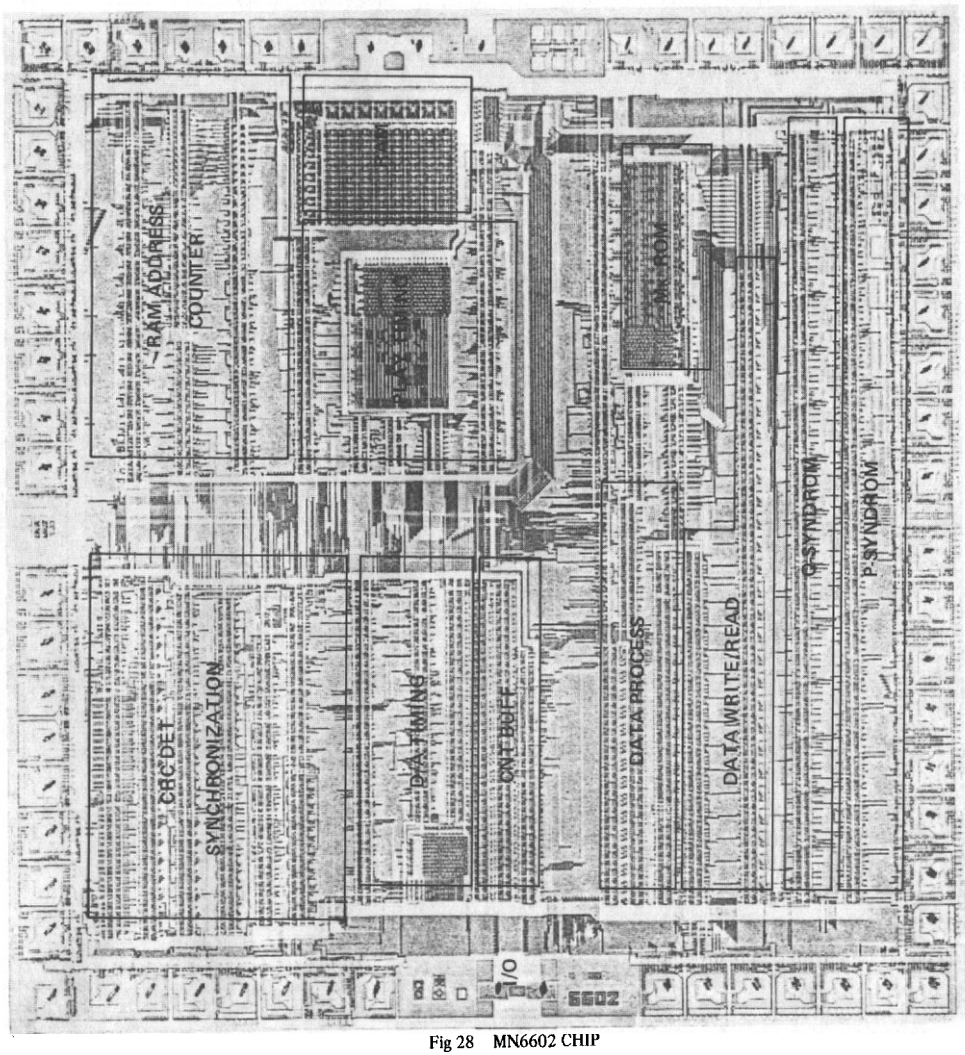


Fig 28 MN6602 CHIP

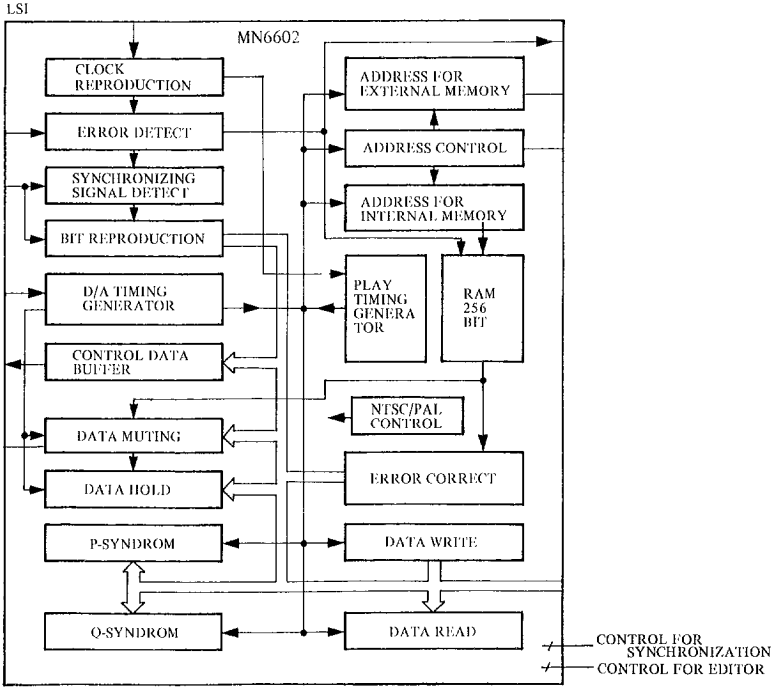


Fig. 29. Block diagram of MN6602

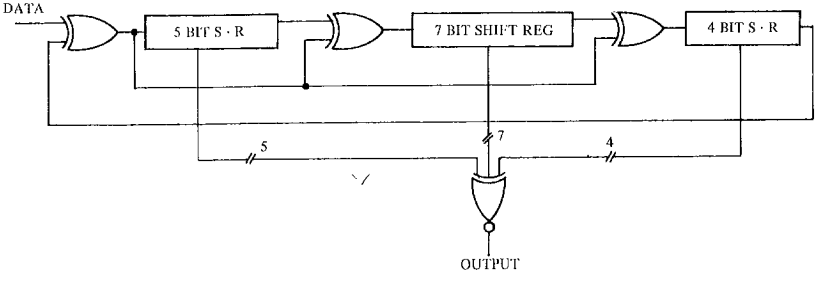


Fig 30 CRC DETECT BLOCK

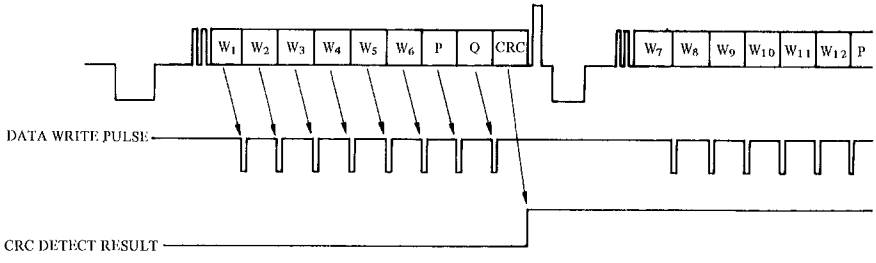


Fig. 31. CRC synchronigation

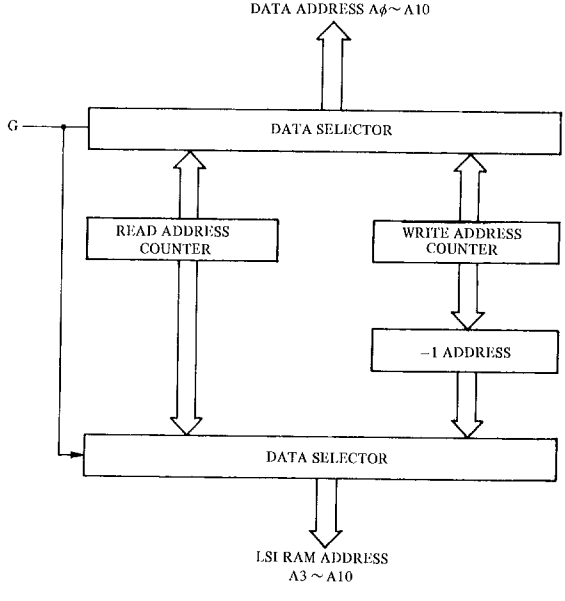


Fig. 32. Adress for LSI RAM and external RAM

M1 =

M2 =

M3 =

M4 =

M5 =

Fig. 33 MK MATRIX

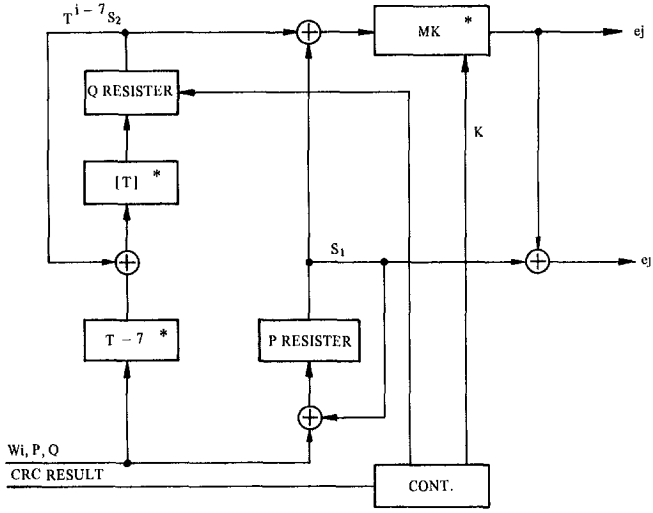


Fig. 34. Block diagram of error correct

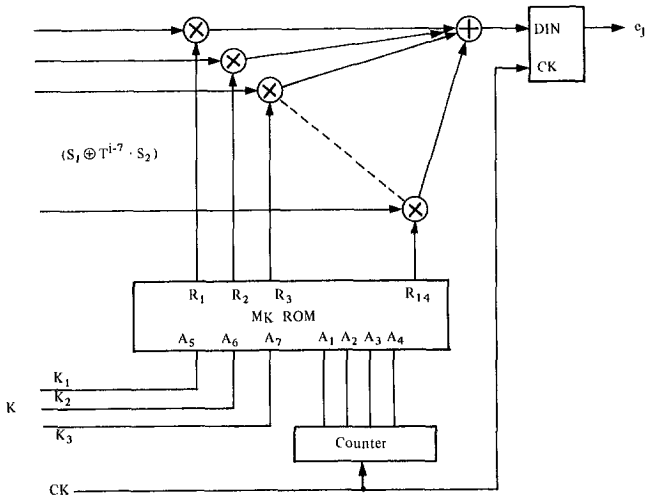
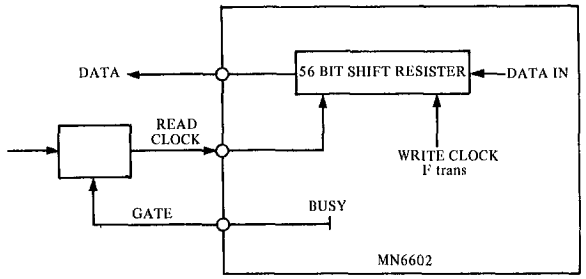
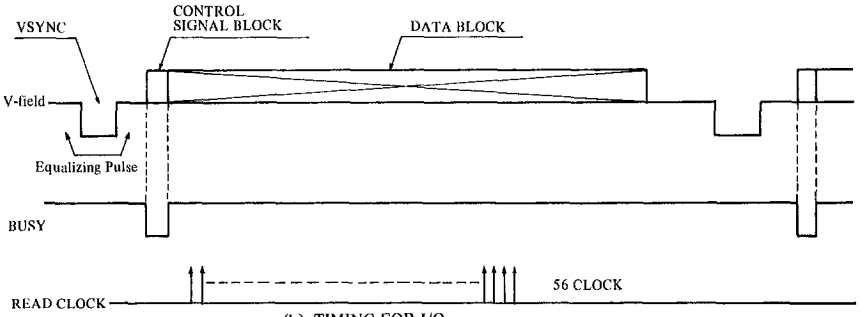


Fig 35 $M_K \cdot (S_1 \oplus T^{i-7} \cdot S_2)$ Processing circuit



(a) I/O BLOCK DIAGRAM



(b) TIMING FOR I/O

Fig 36 I/O FOR CONTROL SIGNAL BLOCK

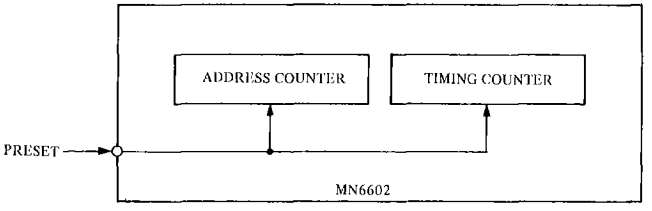


Fig 37 PRESET FOR SYNCHRONIZING

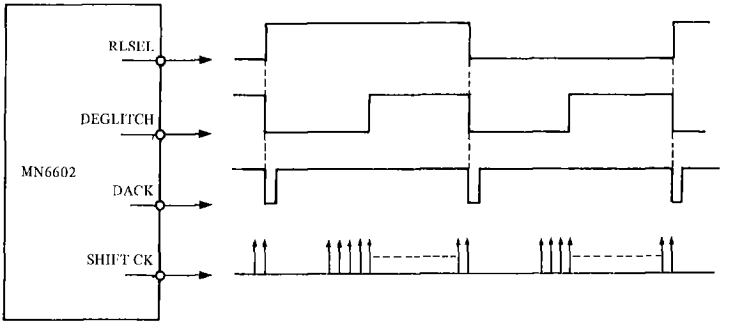


Fig 38 TIMING FOR D/A CONVERTER

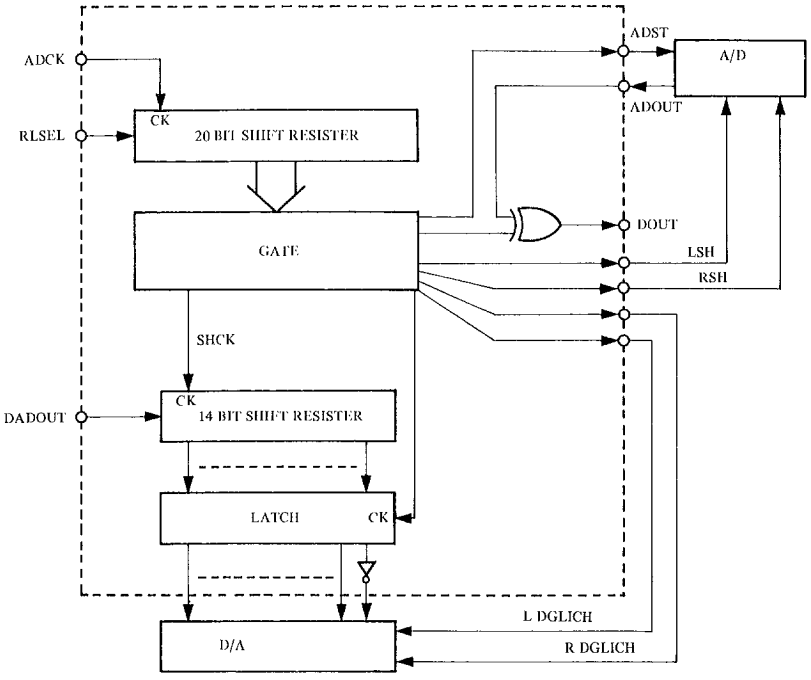


Fig. 39. BLOCK DIAGRAM OF AN6860

Table 3 Basic specifications of IC AN6860

PROCESS	IIL
I/O	TTL COMPATIBLE
GATE NO	1092
CHIP SIZE	4.0mm x 4.6mm
MAX. FREQUENCY	Tpd 25ns/GATE
PACKAGE	28 PIN DIL

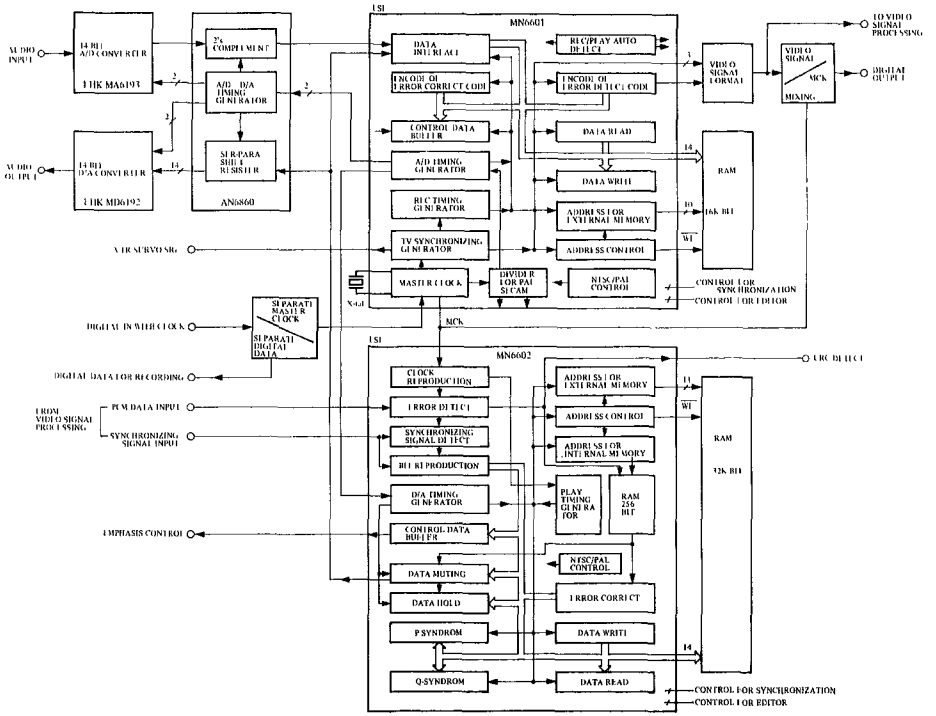


Fig. 40. Digital Processing Block