Signal Processing on an Experimental Digital Audio Tape Recorder

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This paper describes the signal processing system of a stationary head digital audio tape recorder (S-DAT). A Galois logic unit (GLU) and a syndrome generator (SND) were developed, as two IC chips, for use in the error correction system. An experimental S-DAT was designed using IC circuitry throughout including these newly developed chips. The circuitry proved to be suitable and practical.

(1) Introduction

The experimental S-DAT employs a tape cassette which is smaller than an ordinary "compact cassette", and features a 20-track thin-film tape head that provides record and playback on a half-width of the tape. Currently under development, due consideration is beinq given to its electrical performance characteristics as well as ease of operation.

The signal processing system was designed for total adoption of LSI circuits, and features the two newly developed GLU and SND chips used in its error correction circuit (ECC) unit. This report covers the excellent results that were obtained.

(2) Functional description

A functional block diagram of the S-DAT is shown in Fig.1.

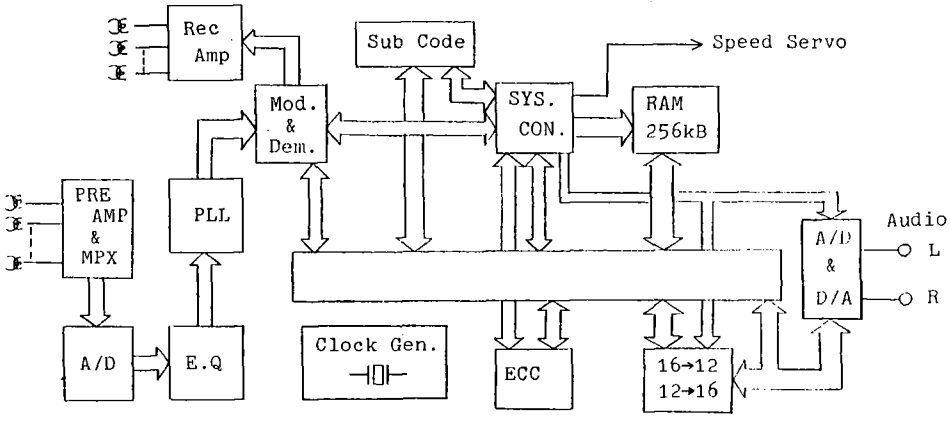

Fig.1 Block diagram of the S-DAT

The signal picked up by each tape-head is amplified by a pre-amplifier and fed into the multiplexer which switches from one head to the next and serializes the signals. The serialized analog signal is converted to a digital signal by the A/D converter, and all subsequent processing is performed digitally. Since the digital processing up to the phase-locked-loop stage has been dealt with in a previous paper(2) an explanation will not be given here.

(3)The system controller unit

A block diagram of the system controller unit (SCU) is shown in Fig.2. The SCU controls the MODEM, the ECC, and the A/D-D/A units in accordance with the S-DAT's operational format. It also performs the interfacing functions between the main memory and the above described peripherals. The SCU normally performs syndrome operations until a request is input from any of the peripherals, then it will halt syndrome operations and start processing according to the request. This interrupt type of operation allows simplification of the hardware since the Time Base Corrector (TBC) circuit becomes unneccessary, while TBC and interleave/de-interleave functions are accommodated by data-mapping on the main memory. This mapping is provided for various interleave formats by changing the MAP ROM.

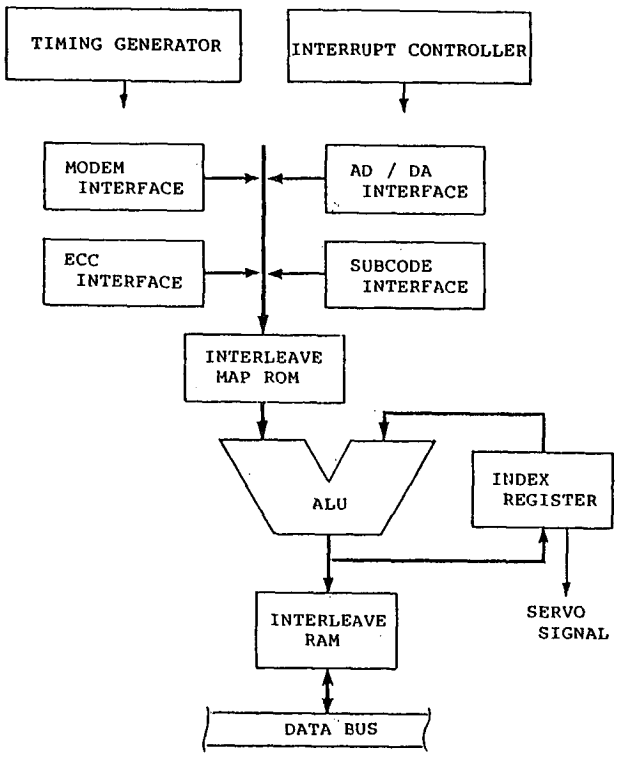

Fig. 2 Block diagram of the system contoller

(4) Signal processing by the ECC

For the detection of errors in the play-back signals, the GLU was adopted and a micro-programming system was implemented. The following describes the GLU, and the syndrome operation unit(SND) both of which constitute an essential part of the ECC, and were successfully made into IC chips by utilizing gate array-technology.

The function of each chip is described in the following.

1. The syndrome operation unit.
Based on the generator polynomial series:

$$G(X) = X^8 + X^4 + X^3 + X^2 + 1$$

when the eight syndrome operations are executed simultaneously on the inputted symbol
and if,

H: parity check matrix
V: received symbol
S: syndrome

then, the contents of the syndrome operations can be represented by,

$$H * V = S$$

If all the components of S are zero, then it can be inferred that the symbol is correct.
The output of the SND is connected to the internal bus of the GLU thus constituting a single system.

2. The Galois logic unit(GLU)
The GLU consists of an arithmetic-logic unit (ALU), a group of accumulators and registers, flag registers for conditional jumps, and a program counter.
The operation unit performs addition/subtraction with $(2^8 - 1)$ as the modulus; it also performs AND, OR, and EX-OR logic operations. Multiplication/division of the Galois field elements is performed by addition/subtraction of exponents expressed as powers of the primitive element "α" . Transformation to the original 'exponent expression' or inverse transformation of the field elements is executed by a transform table containing ROM.
This 'table' also was made to contain the solutions to the quadratic polynomial expressions of error locations, in order to reduce the error correction processing time.
Two accumulator/register groups each comprised of 4 accumulators and 10 registers have been provided, giving adequate storage capacity for handling other digital audio applications.
Additionally, the internal data bus is provided with external connection pins to enable expansion of the ECC's syndrome ALU, working RAM, and I/O ports.
Control of the GLU is performed by a 24-bit microinstruction program, and each command is executed by a 5MHz clock cycle.
The program counter unit, in addition to showing the arithmetic results, performs such functions as: condition jump initiated by external flags, call/return of single level subroutines, and selection of start address after reset.

The architecture of the ECC using these two chips is shown in Fig. 3. Expansion of the program ROM, table ROM, working RAM, and output ports, is made possible by expansion ports. Also considerations for connecting digital equipment other than DATs have been made.
A development support system has been provided in order to facilitate the developing of source and object programs.

- o An editor program has been made available.
- o A cross assembler program is available for object program development.
- o A tracer is available for simulation.

For debugging application programs, the cross assembler enables checking of grammatical errors, after which the tracer simulates the operation of the hardware, permitting complete checking and subsequent elimination of any bugs.

As an example, when this system is used for the error correction in DATs, double error correction can be performed in approximately 70 steps per series, and even in the case of octuple erasure correction approximately 530 steps per series was found to be sufficient.

The above proves that the system's performance is adequate for practical purposes.

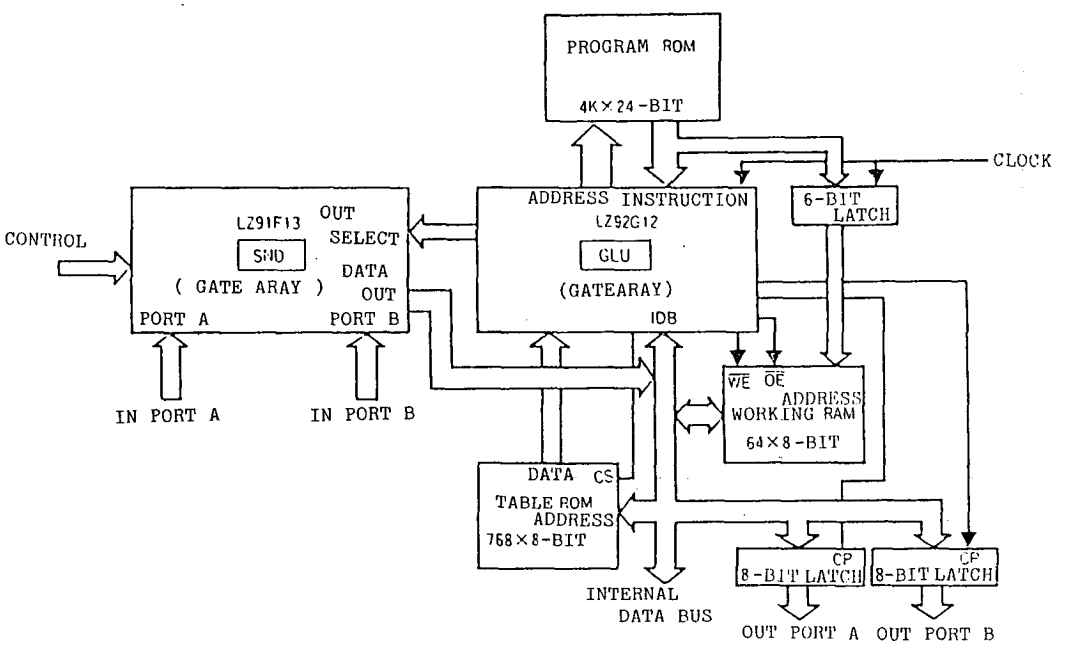

Fig. 3 Block diagram of the error correction circuit

(5) Conclusion

The signal processing system adopted for the experimental stationary head digital audio tape recorder was almost completely digital throughout, and its circuitry was proved to be both suitable and practical for large scale integration. The S-DAT format includes a cue track, sub-codes and ID codes, and other new applications are anticipated in the future. Additionally, the LSI-set lends itself to other applications such as R-DAT, CD, CD-ROM, erasable-disk, and still-camera systems. The LSI-set can be utilized effectively in any digital device that employs Reed Solomon code error correction circuitry.

References:

(1) Miyauchi, Kichira, et al. "Thin Film Heads for Audio use." 33rd Applied Magnetics Society Convention. Data 33-5 P.35 (1984)

(2) Sugita, et al. "A Method for Sensing Data in Stationary Head Digital Tape Recorders." The Institute of Electronics and Communication Engineers of Japan. Technical Report EA 82-59, Pages 33-40 (1982)