PROFESSIONAL-USE PCM AUDIO PROCESSOR WITH A HIGH EFFICIENCY ERROR CORRECTION SYSTEM

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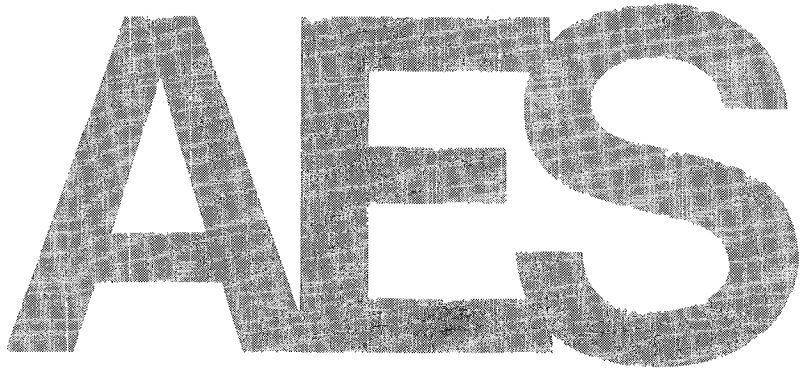

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Abstract

A digital signal processor for professional use 2-channel PCM (Pulse Code Modulation) recording system utilizing 3/4-inch cartridge type VTRs will be described in this paper. The basic system consists of the processor, two VTRs, an editor and a delay unit.

To ensure its professional-use quality, a powerful coding system of 16-bit linear quantization having ample correctability against transmission errors and flexible editing capability is applied. The transmission bit-rate is kept low well within the capacity of 3/4" VTR, furthermore, the coding is devised to enable a stable timing control of data input and output. As a result, the processor is practically fault-free of error correction.

For editing recorded tapes, an electronic editing is inevitable for various reasons, VTR's herical-scan format is one of them. The authors have designed two types of electronic editing methods on this system. One is "simple editing" which combines two digital signal flows reproduced from two VTRs by switching between the two at a rate of pseudo-TV frame (approx. 33m sec. per frame unit). In this editing,

some discontinuity of the decoded waveform is admitted. The other is the "high precision editing" defined by authors, for which an electronic editing unit has been newly developed. The unit smooths out such waveform discontinuity by providing each signal flow with appropriate weighting done digitally.

Introduction

A major use of professional type 2-channel PCM-recording system are stereophonic recording, editing and disc mastering.
Especially in the editing, more than 10 hours of operation is quite common, which imposes high reliability to the system, thus extraordinary high error correctability is required. As well known, mass of digital data is processed at a high transmission bit-rate which tends to generate data error in the PCM recording system resulting unpleasant noise. From this viewpoint, an effective error correction scheme is important, and to the VTR applied PCM system, the problem is more serious because of its irregular data transmission through the pseudo-TV signal.

On the other hand, a 2-channel PCM recording system may be operated in conjunction with other professional audio equipment such as editing console, disc record cutting system, etc. Accordingly, additional requirements are also imposed, such as provisions of analog and digital signal input-output, or synchronization capability with other equipment.

Required functions and possible applications of the processor

(1) PCM recording of stereophonic signal from an analog mixing console.
(2) 2-channel digital recording from multi-channel digital recorder through digital mixing console, a sampling frequency conversion where necessary.
(3) Digital tape dubbing.
(4) Quartz locked timing reproduction.

(5) Simple editing with variable speed monitoring.
(6) High precision editing with the exclusive editor.
(7) Disc mastering with a digital delay unit for preview.

Coding Configuration

To satisfy the aforementioned operational functions, applications, and sound quality for professional use, the following provisions are imposed to the processor design:

(1) Sampling Frequency: 44.056 KHz
The figure enables to have an audio bandwidth up to 20 KHz, and to transform the signal to video compatible.

(2) Quantization: 16-bit Linear
16-bit linear quantization with binary number in 2's compliment.

(3) Error Correcting Code:
A highly effective error correcting code called "Triple Error Correcting Code with Error Pointers" is adopted. The code is capable of correcting three occasionally generated errors within any field. This ensures high recording reliability.

(4) Transmission bit-Rate: 3.084 Mbits/sec.
This is to form the pseudo-TV signal compatible with VTRs, and to constitute the highly reliable code at a low transmission bit-rate.

(5) Editing Capability:
Application of block coding per field, block address and local field address, enables the simple editing with variable speed monitoring, and the direct field address system for the precision editing is employed.

Construction of the Processor

Fig. 1(a) shows the diagram of the recording section of which the operation timing is controlled by the built-in quartz oscillator, when the inputs are analog signals. The field address code is generated by counting the field of the pseudo-TV signal, and is represented by 6 digits in BCD-code (24 bits). The value of this address code approximates the time length of the recorded segment.

When the input signals are digital, the outputs of the quartz oscillator, the A/D converters and the field address counter are switched to the digital inputs fed from interfaced units. An exception is that the built-in quartz oscillator is used to control system's timing when the recording system is driven synchronized with other systems, conducting the high precision editing for example.

Fig. 1(b) is the diagram of the recording section. In this section, the synchronizing pulse is separated from the input signal (Pseudo-TV signal). Detected digital data are error checked and corrected (if necessary), and are sent out from the output terminal with an appropriate timing control. This digital output is accompanied by the address code and the frame synchronization signal. The D/A converters are independent from other circuits, so that it can be used for monitoring digital signals such as editor output.

Signal Formats

(1) Recording Signal

Fig. 2(a) and (b) show the recording signals to a VTR. Each of them corresponds to the even or odd field signal. Hc_1 and Hc_2 are "Control Signal Blocks", which contain the field address code and the control signals. $Ho \sim H_{244}$ are "Data Signal Blocks", which consist of the data words and the associated error correcting words. The block marked "White ref." is the white color reference signal to optimize the AGC operation of VTR.

Fig. 3(a) and (b) are the constructions of Hc_1, Hc_2 and $H_0 \sim H_{244}$. In the control signal block Hc_1 or Hc_2, "Ac" is a block address word which consists of 2 bits of the block identification code and the local field address code in the same number of bit. "FA" stands for the field address code which is represented by 6 digits in BCD-code (24 bits) and is equally contained both in Hc_1 and Hc_2. 112 bits capacity of blank space is provided for user's optional codes which may be program identification code, control code, etc. "C" is the error detection word having 22 bits for block signal.

In the data signal block, shown in Fig. 3(b), "An" is a block address word of 12 bits. The word consists of 2 bits of block identification code, 2 bits of local address code, and 8 bits of block number code which corresponds to the block suffix. Two sets of three words symbolized as W_{even} and W_{odd} are 16-bit quantized audio signals obtained by sampling the two analog inputs of Channel L and R. Two words P_1, P_2 are error correcting word generated by data words and C is the 22 bit error detection word (CRCC). The generation algorism for P_1 and P_2 will be described later. Error correction is conducted by using the error detection result as error pointers.

Fig. 4(a) and (b) show the compositions of block address words "Ac" and "An". And Table-1 shows the functional assignment of "BIC" (Block identification code). As to the "LFA" (Local Field Address), the same value is given to all the blocks within the field.

(2) Interfacing

The formats of digital input/output signals are shown in Fig. 5 (a) through (f), and interfacing should be in accordance with the formats. In this figure, (a) is the clock pulses of 3.084 MHz, (b) is the data word synchronizing pulses of 44.056 KHz which is equal to the sampling frequency. (c) and (d) show the composite signals consist of the data word of quantized audio signal obtained by sampling channel L or R input, also data word synchronizing pulse and odd-parity check bit. (e) shows the composite signal which consists of the field address code "FA", the identification code "DIC", the field synchronizing pulse, and odd-parity check bit. (f) is the frame synchronizing pulse.

The transmission bit-rate of foregoing composite signals (c) $\sim$ (e) is set at 3.084/2 Mbits/sec. to ensure high reliability for professional recording. All of the six signals are necessary when carrying out digital dubbing or high precision editing, and the four signals of (a) $\sim$ (d) are necessary to drive D/A converters.

An interfacing diagram to transmit those digital signal is illustrated in Fig. 6. The level of those signals should be TTL/2 at the receiver input terminals, and coaxial cable of 50 ohm under this condition, transmission distance of several tens of meter is possible.

Encoding

Fig. 7 shows the encoding diagram of the data blocks, where "D^{ℓ}" represents the delay of ℓ words. For example, $D^{\ell} \cdot W_{6n+1}$ is equal to $W_{6n+1-6\ell}$. The generation algorisms for the error correcting words P1 and P_2 are as follows:

$$P_{1,6n} = W_{6n} \oplus W_{6n+1} \oplus W_{6n+2} \oplus W_{6n+3} \oplus W_{6n+4} \oplus W_{6n+5} \quad \cdots(1)$$

$$\begin{aligned} P_{2,6n} &= D^{0} \cdot W_{6n} \oplus D^{4} \cdot W_{6n+1} \oplus D^{8} \cdot W_{6n+2} \oplus D^{12} \cdot W_{6n+3} \\ &\quad \oplus D^{16} \cdot W_{6n+4} \oplus D^{20} \cdot W_{6n+5} \oplus D^{24} \cdot P_{1,6n} \\ &= W_{6n} \oplus W_{6n+1-24} \oplus W_{6n+2-48} \oplus W_{6n+3-72} \\ &\quad \oplus W_{6n+4-96} \oplus W_{6n+5-120} \oplus P_{1,3n-144} \quad \cdots(2) \end{aligned}$$

In these equations, " $\oplus$ " stands for the addition among the vectors (W, P_1, P_2) over GF(2) (Galois field of two elements). For grouping the coding within unit field, every suffix number attatched to each word in Eq.(1), Eq.(2) is given as the number modulo 1470 (the residue divided by 1470). Consequently, suffix number of each block becomes the number modulo 245. Table 2 shows the relationship between sampling timings, words, word displacement using delay operator "D" and block numbers.

The symbol "$\mathbf{x}G_1$" represents the generation of error detecting word "C" within unit block, and the same algorism is applied to generate the error detecting word within the control signal block and the data block. As explained earlier, the size of each block is 162 bits, and bit segment is named "bn". Suffix "n" increases toward the block end. The information (the words of An through P_2 in Fig. 3) occupies $b_1 \sim b_{140}$, and the error detecting word C occupies $b_{141} \sim b_{162}$. These information and C can be represented in polynomial expression I(x), and C(x), where x is a indeterminant:

$$\text{Information: } I(x) = b_1 \cdot x^{161} + b_2 \cdot x^{160} + \ldots + b_{140} \cdot x^{22} \quad \ldots(3)$$

$$\text{C} \quad : C(x) = b_{141} \cdot x^{21} + b_{142} \cdot x^{20} + \ldots + b_{162} \cdot x^{o} \quad \ldots(4)$$

C(x) is the residual polynomial obtained by deviding the I(x) by generating polynomial G(x), and I(x) is modified prior to this operation. Mathematically, C(x) is expressed as follows:

$$C(x) = (1 \oplus b_1) \cdot x^{161} + \ldots + (1 \oplus b_{22}) \cdot x^{140} + b_{23} \cdot x^{139} + \ldots\ldots + b_{140} \cdot x^{22} \pmod{G(X)} \quad \ldots(5)$$

where

$$G(x) = x^{22} + x^{9} + x^{5} + x + x^{o} \quad \ldots(6)$$

Decoding and Error Correcting

(1) Decoding Method

Among several alternative ways of decoding, we adopted the way shown in Fig. 8 for highly effective error correcting capability in practical use. "$\mathbf{x}G_0$" represents a error checking operation by "C", and the result are used as error pointers in the error correcting operations. After the error detection, the words are written in the memories in accordance with the block address word, in turn the words are read out of the

memories recovering to the original arrays of the "P_2" generated and the"P_1" generated respectively, and errors if produced are corrected.

The principle of error correction is that if only one word among the 8 words of Eq. (1) or the 7 words of Eq. (2), is labeled error with a error pointer, the erroneous word will be calculated (corrected) as the solution of a linear equation. Now the error corrections using the Eq. (1) and the Eq. (2) are designated the "P_1-correction" and the "P_2-correction" respectively. The followings are examples of the P_1-correction and the P_2-correction when the W_{6n+1} is error labeled:

P_1 -correction:

$$W_{6n+1} = P_{1,6n} \ominus W_{6n} \ominus W_{6n+2} \ominus W_{6n+3} \ominus W_{6n+4} \ominus W_{6n+5}$$

$$= P_{1,6n} \oplus W_{6n} \oplus W_{6n+2} \oplus W_{6n+3} \oplus W_{6n+4} \oplus W_{6n+5} \cdots (7)$$

P_2 -correction:

$$W_{6n+1} = D^{-4} \cdot (P_{2,6n} \ominus W_{6n} \ominus D^{8} \cdot W_{6n+2} \ominus D^{12} \cdot W_{6n+3} \ominus D^{16} \cdot W_{6n+4} \ominus D^{20} \cdot W_{6n+5} \ominus F^{24} \cdot P_{1,6n})$$

$$= D^{-4} \cdot P_{2,6n} \oplus D^{-4} \cdot W_{6n} \oplus D^{4} \cdot W_{6n+2} \oplus D^{8} \cdot W_{6n+3} \oplus D^{12} \cdot W_{6n+4} \oplus D^{16} \cdot W_{6n+5} \oplus D^{20} \cdot P_{1,6n} \cdots (8)$$

where " $\ominus$ " is a subtraction of vectors over GF(2) and is same as $\oplus$.

Decoding manner of Fig. 8 is as follows, the P_2-correction(1) is performed first, then the P_1-correction(1) taking the result of P_2-correction(1) into account, subsequently, the P_2-correction (2) is operated carring the preceding results into effect, and so on. Thus it can be said that this decoding is a feed back decoding. If error detection mistake is made using C, it will be still detectable and correctable provided that the most of other blocks of the field are not erroneous. Unless all the 8 words in the Eq.(2) are erroneous, the sum of the 8 words in Eq.(2) is 0, but when errors are not detected,

sum will not be 0. For example, when W_{6n} contains undetected error, the sum S_2 is expressed as follows:

$$S_2 = D^0 \cdot (W_{6n} \oplus E) \oplus D^4 \cdot W_{3n+1} \oplus \cdots\cdots \oplus D^{24} \cdot P_{i,6n} \oplus P_{2,6n}$$
$$= E \neq 0 \qquad \cdots(9)$$

where E is the error vector contained in W_{6n} and S_2 is a syndrome.

When S_2 is not 0, all the 8 words should be labeled error as the erroneous word can not be identified, and the words will be corrected later by the P_1-correction(1), etc.

(2) Error-Correction Capability

In case erroneous blocks which are less than 4 in a field have been labeled with C without fail, the words in the blocks can be error-corrected, accordingly this coding is to say a triple error correcting code system. If erroneous blocks happen to be more than 3 in a field at particular location, the errors will not be corrected, as explained in the following.

When more than 1 erroneous words are included in the 8 words of input, the error can not be corrected by the P_2-correction(1). In other word, when one word is observed error and one more erroneous word exists in the remaining 7 words, the P_2-correction (1) is no longer capable. Accordingly, if the error rate of the input to the P_2-correction(1), which is a block error rate, is given as p_H, $p_\varepsilon(p_2)$, theprobability of incorrectness, is expressed as follows:

$$p_\varepsilon(p_2) = p_H \cdot ({}_7C_1 \cdot p_H \cdot (1-p_H)^6 + \cdots + {}_7C_7 \cdot p_H^7)$$
$$\doteqdot 7 \cdot p_H^2 \qquad (10)$$

The same is true to the P_1-correction(1) with 7 words instead of 8 words. Hence, where error rate of the words of the input is $p_\varepsilon(P_2)$ and the processes of $p_\varepsilon(P_2)$'s are independent each other *1), $p_\varepsilon(P_2, P_1)$, the probability of incorrectness becomes:

$$p_\varepsilon(P_2, P_1) \fallingdotseq 6 \cdot p_\varepsilon^2(P_2) \fallingdotseq 294 \cdot p_H^2 \qquad (11)$$

The processes of subsequent P_2-correction(2) and P_1-correction (2) are dependent on the precedings and involves complex calculations. $p_\varepsilon(P_2, P_1, P_2, P_1)$, the probability of incorrectness in the P_1-correction(2) is given as follow:

$$p_\varepsilon(P_2, P_1, P_2, P_1) \fallingdotseq 21 \cdot p_H^4 \sim 30 \cdot p_H^4 \qquad (12)$$

where values vary depending on the words ($W_{6n} \sim W_{6n+5}$).

If the error-correction was performed only with the error-pointers using C, the probability of Eq.(12) is realized with P_1-correction(1), P_2-correction(2) and P_1-correction(2). And the P_2-correction(1) in the Fig. 8 may be omitted. Our actual measurement yielded p_H of $5 \times 10^{-6} \sim 10^{-4}$. If p_H is deemed less than 10^{-4}, the expected value of incorrectness N_ε is *2):

$$N_\varepsilon < \overline{p}_\varepsilon(P_2, P_1, P_2, P_1) \times 44056 \times 2 \times 3600 \fallingdotseq 10^{-6} \quad \text{(words/hour)} \qquad (13)$$

where $\overline{p}_\varepsilon(P_2, P_1, P_2, P_1)$ is a mean value of $21 \cdot p_H^4 \sim 30 \cdot p_H^4$

Other probable incorrectness occasions take place in the following two cases:
(a) When a burst error occurs for period of more than 37 μ more than one out of 8 words in the P_2-correction, and more than one out of 7 words in the P_1-correction become

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*1) see appendix 1
*2) see appendix 2

erroneous even with the effects of the preceding corrections. Consequently, error-corrections are not completed. However, in our examinations, such occasion has never occured.

(b) In case the error-detection with C fails and there exists other errors detected in particular locations, error-corrections cannot be completed. The probability of such detection failure $P_{f(C)}$ is:

$$P_{f(C)} = p \times 2^{-22} \quad \ldots.(14)$$

then, the probability of incorrectness $P_{\varepsilon(C)}$ is:

$$P_{\varepsilon(C)} \doteqdot K \times p_H^2 \times 2^{-22}$$

where K is constant smaller than 245. ....(15)

As p_H is less than 10^{-4}, the expected incorrectness is less than 3×10^{-5} (cases/hour). It should be noted that error detection is performed not only by "C" but also by the block address word An. If an error-period of a block is shorter than 23 bits, the failure of detection will not occur. Thus the total probability of the failure is far smaller than Eq. (14) and the expected incorrectness in this case should be far smaller than Eq. (15).

Variable Speed Playback Monitoring

Variable speed playback for the purpose of simple editing is performed by means of the field unit coding, local field address and block number coding systems. The reproduced sound comprises a series of waveforms which are periodically discontinuous at a rate of field, and each waveform is subjected to interpolation errors.

The video output signal from a rotary-head VTR operated at off standard tape speed, contains a bar-noise which extend to several tens of horizontal-period, and mixture of data from two adjacently located tracks. This due to the fact that the

head is no longer scans one track at a time but across multiple tracks. Despite this, the desired field information can be detected by identifying its local field address code, and stable timing control is secured by reading the block number code. Consequently, some incorrectness may happen but no signal processing error is involved in the reproduced sound.

Not yet applied though, a very stable half speed reproduction without data error for disc cutting is possible with this system using a sampling frequency of 22 KHz which reads each field signal twice.

Conclusion

The processor has been developed as a component of the 2 Channel PCM Mastering System which includes an editor and a digital delay unit in addition to the processor. As a professional equipment, the processor assures stable high quality reproduction of sound in prolonged use such as for editing operation. Using this processor, it is quite probable that digitally recorded master tapes are refreshed without any degradation for long term storage because of the processor's powerful error correction capability. By imposing a periodic refreshment procedure for the master tapes to be preserved, the recorded music will become invariable heritage to the future generations.

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Appendix 1

In this appendix, the independance between the two error correcting processes of P_2-correction, and P_1-correction will be discussed. By using the delay operator D, the generation of the error correcting words P_1, P_2 (expressed with Eq. (1) and Eq. (2) in the text), and the construction of the data block Hn is generally expressed as follows.

$$P_{1,6n} = D^{0} \cdot W_{6n} \oplus D^{\rho} \cdot W_{6n+1} \oplus \cdots \oplus D^{\rho} \cdot W_{6n+5} \tag{A1-1}$$

$$P_{2,6n} = D^{0} \cdot W_{6n} \oplus D^{\iota} \cdot W_{6n+1} \oplus \cdots \oplus D^{5\iota} \cdot W_{6n+5} \oplus D^{6\iota} \cdot P_{1,6n} \tag{A1-2}$$

$$H_n = (D^{0} \cdot W_{6n}, D^{\bar{\iota}+\bar{\rho}} \cdot W_{6n+1}, \cdots\cdots D^{6(\iota+\bar{\rho})} \cdot P_{1,6n}, D^{7\bar{\rho}} \cdot P_{2,6n}) \tag{A1-3}$$

$$H_n = \bar{D}^{n} \cdot H_0 \tag{A1-4}$$

where ι , and $\bar{\rho}$ are integers, and in the text, $\iota = 4$, $\bar{\rho} = 29$ are the conditions. Thus the m'th word in the block Hn is expressed.

$$\bar{D}^{m(\iota+\bar{\rho})} \cdot W_{6n+m} = \bar{D}^{n} \cdot \bar{D}^{m(\iota+\bar{\rho})} \cdot W_m \triangleq \bar{D}^{n} \cdot \bar{D}^{mk} \cdot W_m \tag{A1-5}$$

where $m = 0 \sim 5$, $k = \iota + \bar{\rho}$

Now, for better comprehension to the independency, let us track back the error correcting process.

First, let us focus on the P_1-correction process. When Hn is erroneous, the words used for the P_1-correction applied to correct the erroneous words $\bar{D}^{n} \cdot D^{mk} \cdot W_m$ in H_n, are as follows.

$$\bar{D}^{n+mk} \cdot (W_0, W_1, W_2, \cdots\cdots W_5, P_{1,0}) \tag{A1-6}$$

These words are contained in a block expressed by the polynomial;

$$\bar{D}^{n+mK} \cdot (D^0 + \bar{D}^K + \cdots\cdots + \bar{D}^{6K}) \cdot H_0 \qquad \text{(A1-7)}$$

Next let us turn our eyes on the P_2-correction process. The words for the P_2-correction on $\bar{D}^{n+mK} \cdot W$ or $\bar{D}^{n+6K} \cdot P_{1,0}$, are expressed as follows.

$$\bar{D}^{n+mK} \cdot \bar{D}^{\ell\bar{\iota}} \; (D^0 W_0, D^{\bar{\iota}} \cdot W_1, \cdots\cdots D^{6\bar{\iota}} \cdot P_{1,0}, D^0 \cdot P_{2,0}) \qquad \text{(A1-8)}$$

where $\ell = 0 \sim 6$.
These words are contained in a block expressed by polynomial;

$$\bar{D}^{n+mK} \cdot \bar{D}^{\ell\bar{\iota}} \cdot (D^0 + \bar{D}^{\bar{\jmath}} + \cdots\cdots + \bar{D}^{7\bar{\jmath}}) \cdot H_0 \qquad \text{(A1-9)}$$

Thus all of the words which are related with each other according to the Eq.(A1-6) and Eq(A1-8), and used for the P_2-correction and the P_1-correction are contained in the block of following polynomial.

$$\bar{D}^{n+mK} \cdot (D^0 + \bar{D}^{\bar{\iota}} + \cdots + \bar{D}^{6\bar{\iota}}) \cdot (D^0 + \bar{D}^{\bar{\jmath}} + \cdots + \bar{D}^{7\bar{\jmath}}) \cdot H_0 \qquad \text{(A1-10)}$$

The condition for the independency between the P_2-correction and the P_1-correction is that 56 kinds of power indexes of the delay parameter D obtained through expanding the Eq.(A1-10) in to power series, do not coincide with each other. These power indexed take following values.

$$-(N_1 \times \bar{\iota} + N_2 \times \bar{\jmath}) \qquad \text{(A1-11)}$$

where $N_1 = 0 \sim 6$, $N_2 = 0 \sim 7$

Moreover, these values are different under modulo 245 because the coding is made within unit field.

Appendix 2

When block errors generate more than three simultaneously at particular locations, there remains multiple uncorrected data words even after the error correction is made. This means that there exist error words more than two both in Eq.(1) and Eq.(2). In order to obtain the uncorrectable words stastistically it is necessary to make above mentioned relationship clear. Here, a "set" of probabilities which give the event that W_i becomes uncorrectable is $Ps(W_i)$, and the total number of the words is N. $P(W)$ is made up of $P_1(W_i)$ ... $P_M(W_i)$ where $P_1(W_i)$ is a disjoint "subset" which does not have any intersection with probability sets of other word W_j ($j \neq i$), and $P_n(W_i)$ is a subset which is the "sum" of the n-ple intersection defined as the product of $P_s(W_i)$ and another "N-1" probabilities,

$$\underbrace{P_s(W_j), P_s(W_k), \cdots P_s(W_x)}_{N-1} \quad (i \neq j \neq k \neq \cdots \neq x)$$

Furthermore, all of $P_n(W_i)$ are disjoint with each other. $P_S(W_i)$ is expressed as

$$P(W) = P_1(W_i) \cup P_2(W_i) \cup \cdots \cup P_M(W_i) \qquad \text{(A2-1)}$$

Thus the probability set P_S(any) and its subsets P_n(any) which give an event that any of the words become uncorrectable, can be represented as follows.

$$P_S(\text{any}) = P_S(W_1) \cup P_S(W_2) \cup \cdots \cup P_S(W_N) \qquad \text{(A2-2)}$$

$$\left.\begin{aligned} P_1(\text{any}) &= P_1(W_1) \cup P_1(W_2) \cup \cdots \cup P_1(W_N) \\ P_2(\text{any}) &= P_2(W_1) \cup P_2(W_2) \cup \cdots \cup P_2(W_N) \\ &\vdots \\ P_M(\text{any}) &= P_M(W_1) \cup P_M(W_2) \cup \cdots \cup P_M(W_N) \end{aligned}\right\} \qquad \text{(A2-3)}$$

In the case of P_n, the amount of uncorrectable words is n, and the maximum of n is M which is always smaller than or equal to N ($M \leqq N$). As an example, the concept of probability-set, its subsets, and intersections are illustrated in Fig. A1 assuming N = 3. In this figure, probability sets of $P_s(W_1)$, $P_s(W_2)$, $P_s(W_3)$ are represented by circles, and every probability set and subset can be expressed by using areas shown as A,B,...G.

$$\left.\begin{aligned} P_s(W_1) &= A \cup D \cup F \cup G \\ P_s(W_2) &= B \cup D \cup E \cup G \\ P_s(W_3) &= C \cup E \cup F \cup G \end{aligned}\right\} \qquad (A2\text{-}4)$$

$$\left.\begin{aligned} P_1(W_1) &= A \\ P_2(W_1) &= D \cup F \\ P_3(W_1) &= G \end{aligned}\right\} \qquad (A2\text{-}5)$$

$$P_s(\text{any}) = A \cup B \cup C \cup D \cup E \cup F \cup G \qquad (A2\text{-}6)$$

$$\left.\begin{aligned} P_1(\text{any}) &= A \cup B \cup C \\ P_2(\text{any}) &= D \cup E \cup F \\ P_3(\text{any}) &= G \end{aligned}\right\} \qquad (A2\text{-}7)$$

$P_s(\text{any})$ and $P_n(\text{any})$ expressed in Eq.(A2-2) and Eq.(A2-3) can be rewritten by using $P_n(W_i)$.

$$P_s(\text{any}) = \sum_{j=1}^{M} P_j(\text{any}) \qquad (A2\text{-}8)$$

$$\left.\begin{aligned} P_1(\text{any}) &= \sum_{i=1}^{N} P_1(W_i) \\ P_2(\text{any}) &= \frac{1}{2}\sum_{i=1}^{N} P_2(W_i) \\ &\vdots \\ P_M(\text{any}) &= \frac{1}{M}\sum_{i=1}^{N} P_M(W_i) \end{aligned}\right\} \qquad (A2\text{-}9)$$

Therefore, E_N, the expectation value of uncorrected words becomes as follows.

$$E_N = \sum_{j=1}^{M} \left(P_j(\text{any}) \times j\right) \qquad (A2\text{-}10)$$

By substituting Eq.(A2-8) into Eq.(A2-10), the following equation is obtained.

$$
\begin{aligned}
E_N &= \sum_{j=1}^{M} \left(\frac{1}{j} \cdot \sum_{i=1}^{N} P_j(W_i) \times j \right) \\
&= \sum_{j=1}^{M} \cdot \sum_{i=1}^{N} \cdot P_j(W_i) \\
&= \sum_{i=1}^{N} \cdot \left(\sum_{j=1}^{M} \cdot P_j(W_i) \right) \\
&= \sum_{i=1}^{N} \cdot P_S(W_i)
\end{aligned}
\qquad \text{(A2-11)}
$$

If all of $P_S(W_i)$ are equal, E_N becomes

$$
E_N = P_S(W_i) \times N \qquad \text{(A2-12)}
$$

As a result, the expectation value of uncorrectable words can be simply calculated by using Eq.(A2-11) or Eq.(A2-12).

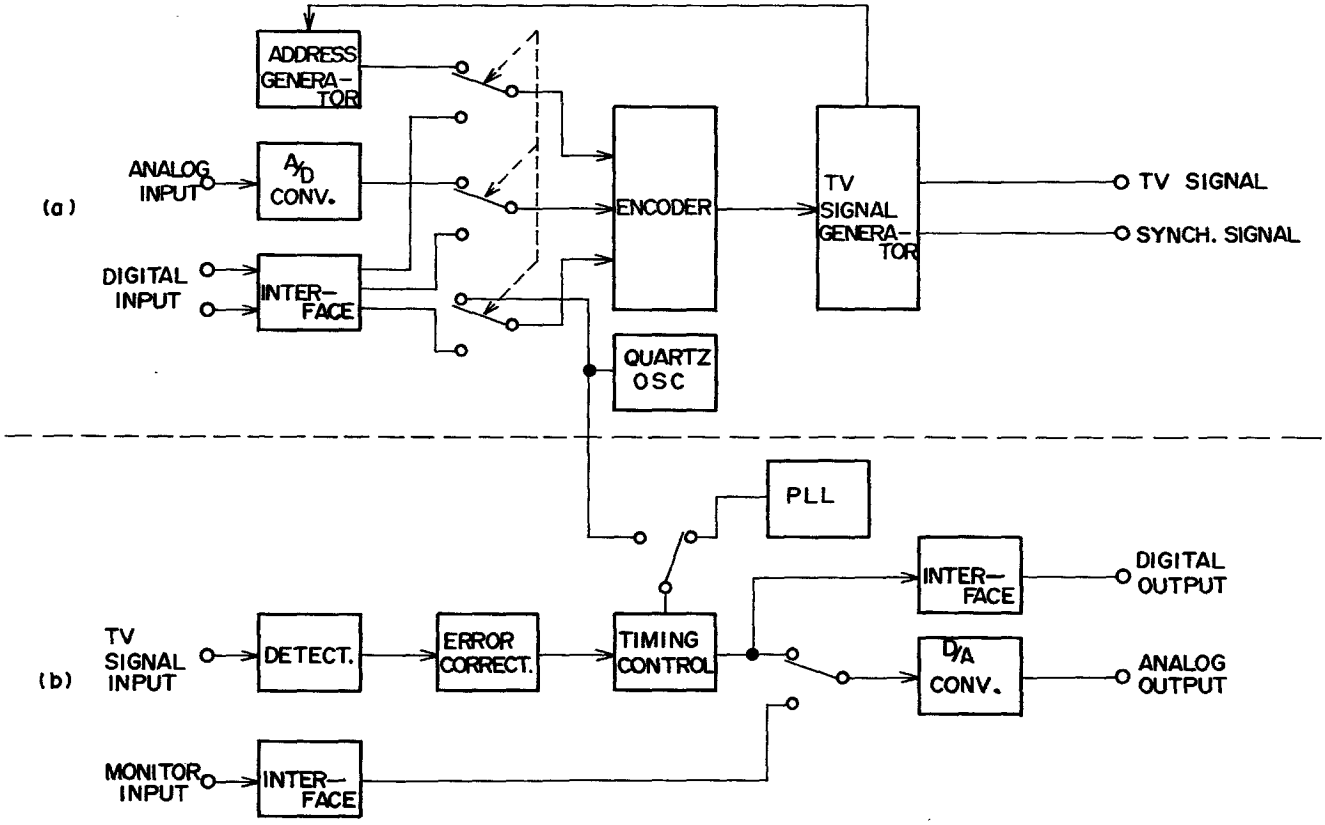

FIG. 1 BLOCK DIAGRAM OF THE PROCESSOR

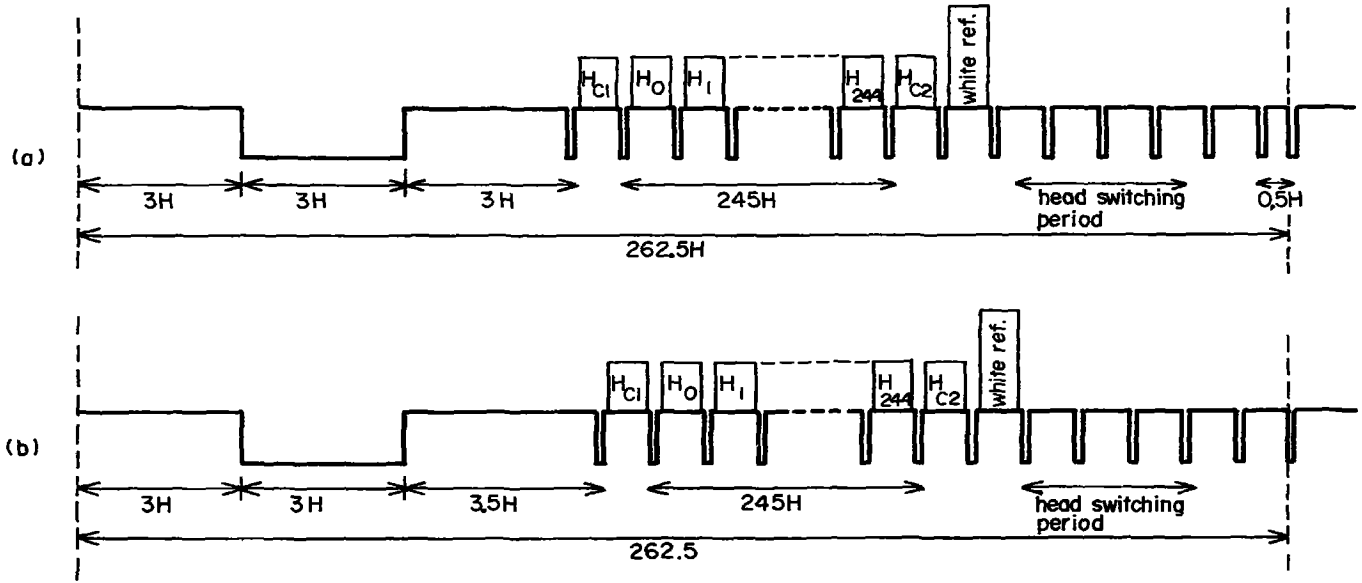

FIG. 2 SIGNAL FORMATS OF EVEN AND ODD FIELDS

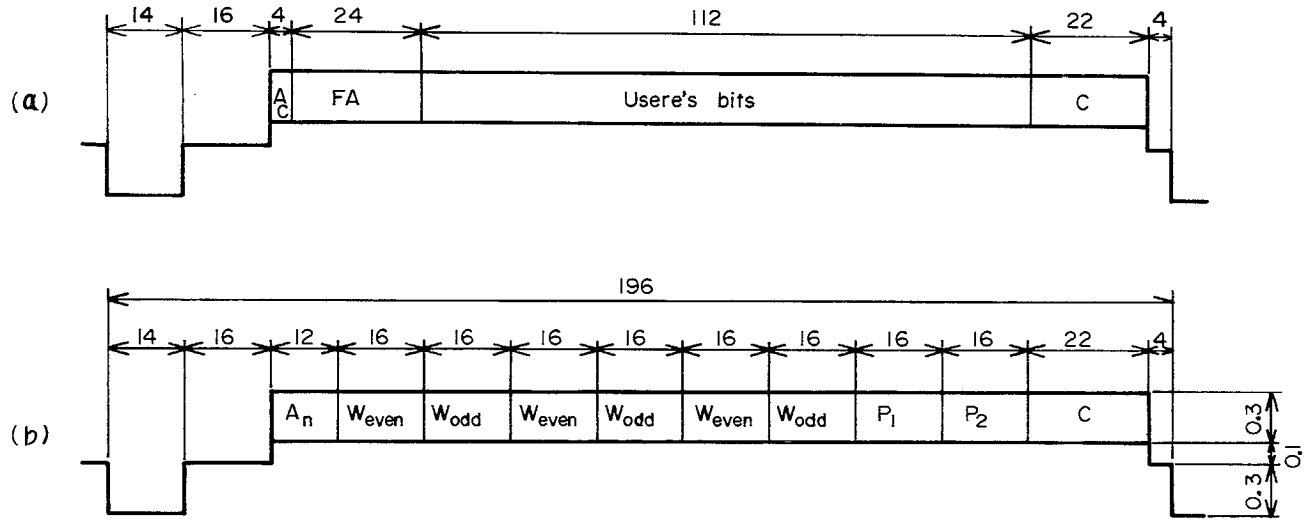

FIG. 3 CONSTRUCTION OF SIGNAL BLOCKS

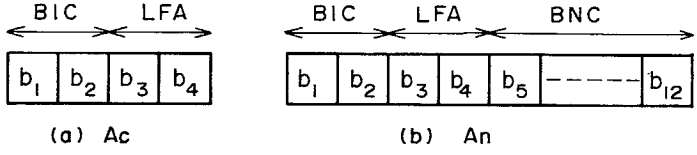

FIG.4 DETAILS OF THE ADDRESS WORDS

b_1	b_2	Assignments
0	0	$H_0 \sim H_{244}$
0	1	H_{C1}
1	0	H_{C2}
1	1	Optional use

TABLE I

BIT ALLOCATION FOR BIC

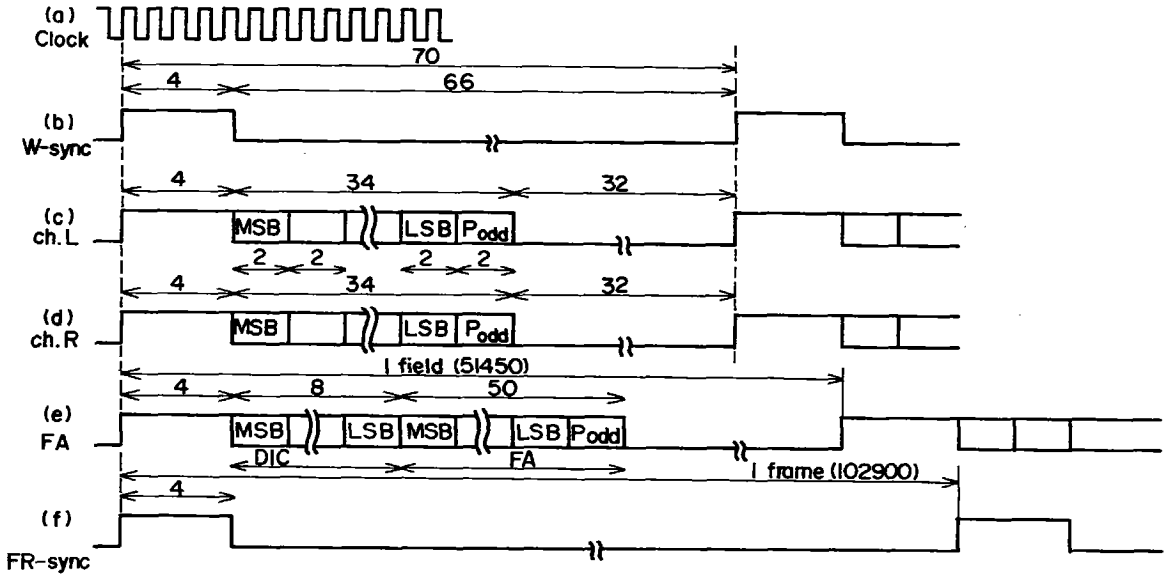

FIG. 5 FORMATS OF INTERFACING SIGNAL

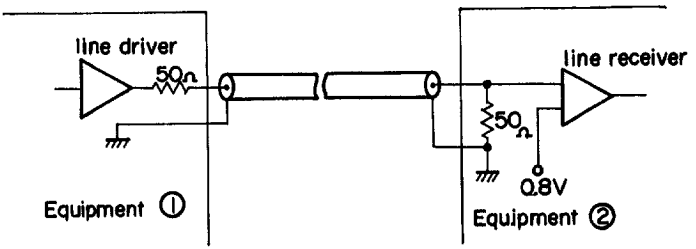

FIG. 6 SIGNAL INTERFACE

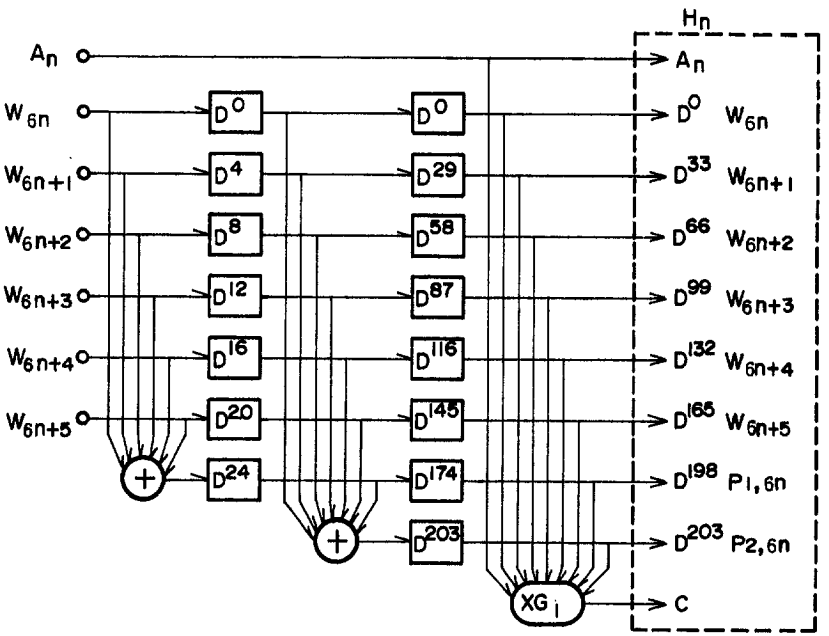

FIG. 7 ENCODING DIAGRAM

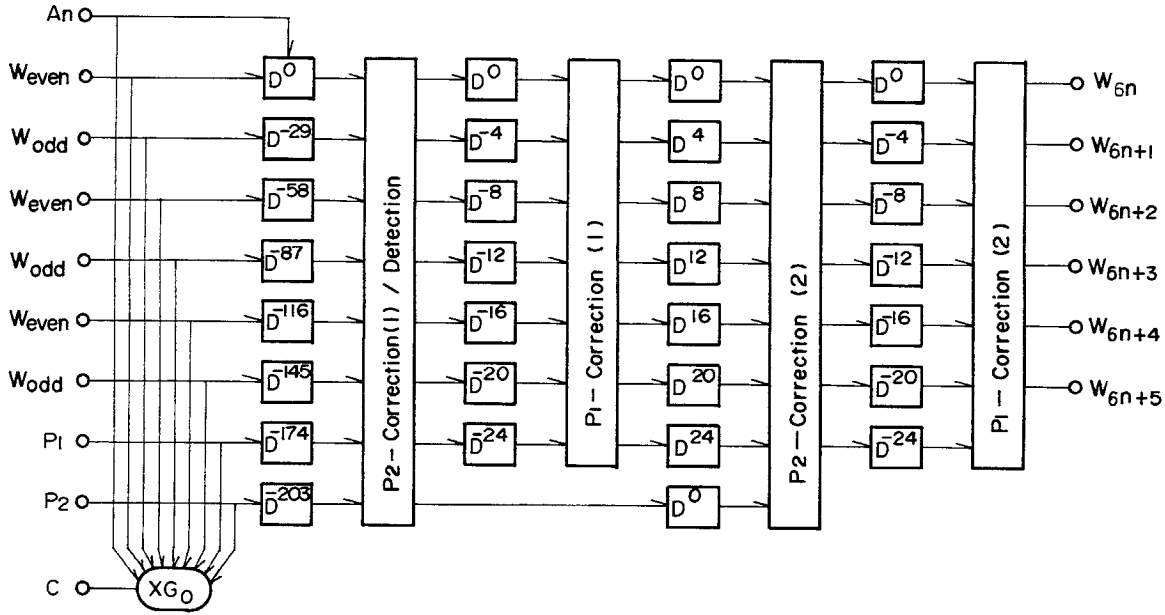

FIG. 8 DECODING DIAGRAM

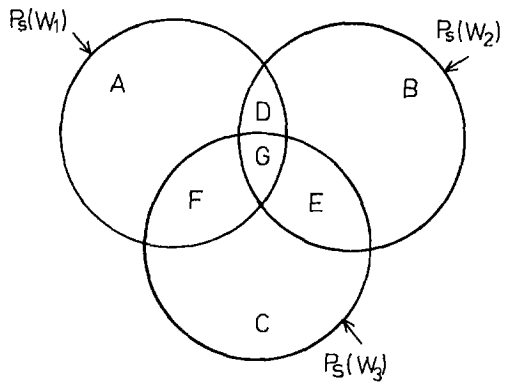

FIG. A1 A MODEL OF SETS & SUBSETS

	sampling time	0	T	2T	3T	4T		731T	732T	733T	734T
L channel	words	W_0	W_2	W_4	W_6	W_8		W_{1462}	W_{1464}	W_{1466}	W_{1468}
	relocated words regarding D	$D^0 \cdot W_0$	$D^0 \cdot W_2$	$D^0 \cdot W_4$	$D^{-1} \cdot W_6$	$D^{-1} \cdot W_1$		$D^{-243} \cdot W_4$	$D^{-244} \cdot W_0$	$D^{-244} \cdot W_1$	$D^{-244} \cdot W_2$
	block to record	H_0	H_{66}	H_{132}	H_1	H_{67}		H_{130}	H_{244}	H_{65}	H_{131}
R channel	words	W_1	W_3	W_5	W_7	W_9		W_{1463}	W_{1465}	W_{1467}	W_{1469}
	relocated words regarding D	$D^0 \cdot W_1$	$D^0 \cdot W_3$	$D^0 \cdot W_5$	$D^{-1} \cdot W_1$	$D^{-1} \cdot W_3$		$D^{-243} \cdot W_5$	$D^{-244} \cdot W_1$	$D^{-244} \cdot W_3$	$D^{-244} \cdot W_5$
	block to record	H_{33}	H_{99}	H_{165}	H_{34}	H_{100}		H_{163}	H_{32}	H_{98}	H_{164}

TABLE 2 DATA LOCATIONS AND TIMING