A PCM DIGITAL AUDIO PROCESSOR FOR HOME USE VTR'S

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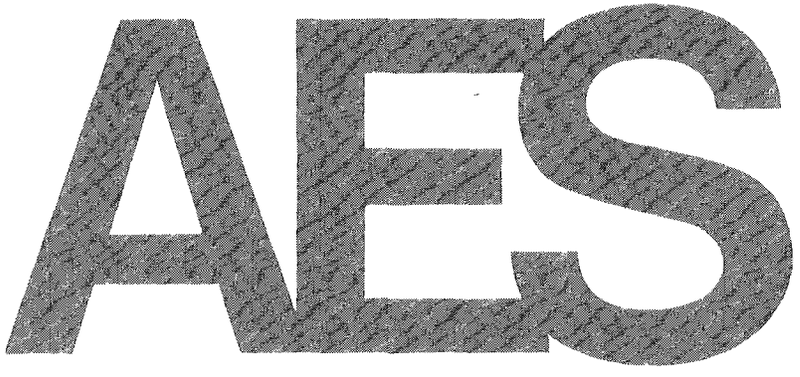

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Abstract

High quality digital audio processor employing extremely effective error correction schemes as an adaptor for VTR's was developed. The format, based on EIAJ standard, features the use of b-Adjacent (8, 6) error correcting code together with CRC. This (8, 6) code can be decoded in more than one way. The authors, after briefing the standard, describe the system designing, coding and decoding, error correction capability, error rate measurement and performance of the processor.

1. Introduction

In the field of digital audio recorders, the standardization has been considered central issue, and long awaited to be settled. In June, 1979, the EIAJ (Electronic Industries Association of Japan) announced the world first standardized format for what is called "a PCM audio adaptor" to be readily connected with any type of VTR's conforming to NTSC television format such as VHS, and β. The description of the standard is incorporated in the EIAJ's technical file STC-007.

The authors have developed a digital audio processor based on this standardized format. This paper includes the outline of the EIAJ standardized format, description of the developed processor, error rate measurement and comments on PAL/SECAM version.

2. Outline of the standardized Format [1]

The standardized format has been decided such that the VTR's, already placed in the market, are readily used without modification as recording media. Accordingly the interface between adaptors (or processors) and VTR's is done in the form of television signal format.
The outline of the standardized format is as follows.

Number of Channels	2 cH
Emphasis (Option)	T_1 = 50 us T_2 = 15 us
Sampling Frequency	44.056 kHz
Quantization	14 bit linear slot
Coding	2's Complement (NRZ)
Transmission Rate	2.643 Mbps
Error Detection	16 bit CRC (CCITT V.41)
Error Correction	b-Adjacent (8, 6) code
Contents of 1 Horizontal line (1H)	Each 3 words for L and R channels 2 words for error correction 16 bit CRC for error detection
Format of 1 field	1H for Control Signal 245H for PCM Data
Interleave	16H Word Interleave
Synchronizing Pulses	Conforming to NTSC
Video I/O Level	1 Vpp
Audio I/O Level	142 mV

2-1 Emphasis

Pre-emphasis is subject to option. The identification code for pre-emphasis is recorded so that the de-emphasis is automatically operated. The emphasis curve is shown in Fig. 1.

2-2 Sampling Frequency [2][3]

As the recording media are VTR's, the choice of sampling frequency should be determined considering the particalur requirements arising from television signal such as sync pulses and head switching. These requirements have been already discussed by the authors and others. However, for references, the review is given.

Choice criteria for the sampling frequency are:

(a) To be able to transmit the audio signal with the bandwidth below 20 kHz.

(b) To be able to convert PCM signal into the TV signal format.

(c) To be able to choose the master clock frequency as low as possible.

(d) To be able to provide enough non-recordable period for vertical sync and head switching.

The relationship between sampling frequency F_S and TV's horizontal sync frequency F_h is,

$$F_S = M \cdot F_h \cdot \frac{525-x}{525} \quad (1)$$

$$= M \cdot F_h \cdot \frac{n}{m} \quad (2)$$

Where M: Total samples per line (1H).
x: Total non-recordable lines per frame.
n/m: Reduced fraction.
F_h = 15.73426...kHz (NTSC line frequency).

For the practical designing of anti-aliasing filter, the value F_S must be chosen greater than 43 - 44 kHz, but not excessively high. The master clock rate F_O is determined as at least the LCM of F_S and $2F_h$, which corresponds to TV's equalizing pulse rate. Accordingly, to get the master clock rate low enough, n and m should be chosen as small as possible. The non-recordable space per frame should be chosen greater than 32H, for incorporating equalizing pulse, vertical sync, and head switching point. Table 1 shows some possible examples of M, x, n, m and F_S.

From this table, taking the above discussion into consideration, we obtain,

M = 3, x = 35, F_S = 44.056 kHz
n/m = 14/15

2-3 Quantization

The standardized format employs 14 bit linear slot system for quantization. Fig. 2 shows the bit arrangement. This allows the use of not only 14 bit linear quantizing but also lower than 14 bit quantizing, regardless of linear or logical companding, with interchangeability kept. It should be noted that logically compressed data must be transcribed into linear representation.

2-4 Transmission Rate [2]

To choose the transmission rate, the following requirements in addition to those in section 2-2 are important.

(e) To be able to use home use VTR's as recording media. (below about NRZ, 3 Mbps)

(f) To be able to get enough redundancy for error correction and horizontal blanking.

Let the transimssion rate be F_C, then,

$$F_C = N \cdot F_h \quad \text{(Kbps)} \tag{3}$$

Where N: Total bits per line (1H).

From equations (2), (3),

$$F_C = N \cdot \frac{1}{M} \cdot \frac{m}{n} \cdot F_S$$
$$= N \cdot \frac{5}{14} \cdot F_S \tag{4}$$

Again, to reduce the master clock rate, N is desired to be the multiple of 14. Based on above discussion, we obtain,

$$N = 168 = 12 \times 14 \tag{5}$$

$$F_C = 2.643 \text{ Mbps} \tag{6}$$

Fig. 3 shows interrelations of clocks.

2-5 Signal Format of Horizontal Line

One horizontal line contains each 3 words from L and R channels, 2 words (P, Q) for error correction, and 16 bit CRC for error detection. The 8 words in 1H, consisting of 14 bits each, constitute b-Adjacent (8, 6) error correcting code. To cope with possible burst errors, each word is interleaved by 16H. Fig. 4 shows the 1H format. Fig. 5 shows interleaving.

2-6 Signal Format of Field

One field contains total of 262.5H out of which 245H is for PCM data transmission called data block and 1H for control signal block. See Fig. 6.

2-7 Control Signal Block

This block contains,

(i) Fixed pattern 56 bits for indicating start of data block in each field. The pattern consists of "1100" repeated by 14 times.

(ii) Content Identification 14 bits

(iii) Address 28 bits

(iv) Control 14 bits
This includes copy-prohibiting code, identification codes for P and Q, and pre-emphasis identification code.

(v) CRC 16 bits

Fig. 7 shows the control signal block.

3. Encoding and Decoding

3-1 Encoding

Two check words P and Q are generated out of every 6 data words according to the relationship,

$$\begin{bmatrix} P_n \\ Q_n \end{bmatrix} = \begin{bmatrix} I & I & I & I & I & I \\ T^6 & T^5 & T^4 & T^3 & T^2 & T \end{bmatrix} \begin{bmatrix} L_{3n} \\ R_{3n} \\ L_{3n+1} \\ R_{3n+1} \\ L_{3n+2} \\ R_{3n+2} \end{bmatrix} \qquad (7)$$

Where n: Integer for indicating the word order.
I: Identity matrix.
T: Companion matrix of the polynomial $1 + x^8 + x^{14}$.

$$T = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

In the equation (7), addition is operated in modulo 2.
Each word is expressed in the form of column vector consisting of 14 bits, in the order of LSB to MSB.
Before transmission the word order is altered from the sequence (L_{3n}, R_{3n}, L_{3n+1}, R_{3n+1}, L_{3n+2}, R_{3n+2}, P_n, Q_n) to (L_{3n}, R_{3n-3D}, $L_{3n+1-6D}$, $R_{3n+1-9D}$, $L_{3n+2-12D}$, $R_{3n+2-15D}$, P_{n-18D}, Q_{n-21D}) by interleaving. From the interleaved words, CRC (Cyclic Redundancy check) charactor is generated to be used as error detection on 1H basis. (See the Fig. 4)
From the equation (7), the check word P is equivalent to even parity.

3-2 Decoding

The received message is checked by CRC. The results of checking are used as error word pointers. To recover the original sequence of the data, the received message with error word pointers is de-interleaved. The equation (7) shows that the check word P is equivalent to even parity. Accordingly, there can be two levels of decoding schemes. One is parity decoding which makes use of the check word P and capable of correcting single word error within one block.

The other is b-Adjacent decoding which makes use of both P and Q, and capable of correcting word errors not more than two within one block. The following shows how the errors are corrected. Now, let the received word sequence (after de-interleaved) be,

$$(L'_{3n},\ R'_{3n},\ L'_{3n+1},\ R'_{3n+1},\ L'_{3n+2},\ R'_{3n+2},\ P'_n,\ Q'_n)$$

Then, the syndromes S_1 and S_2 are defined as,

$$\begin{bmatrix} S_1 \\ S_2 \end{bmatrix} = \begin{bmatrix} I & I & I & I & I & I & I & 0 \\ T^6 & T^5 & T^4 & T^3 & T^2 & T^1 & 0 & I \end{bmatrix} \begin{bmatrix} L'_{3n} \\ R'_{3n} \\ L'_{3n+1} \\ R'_{3n+1} \\ L'_{3n+2} \\ R'_{3n+2} \\ P'_n \\ Q'_n \end{bmatrix} \quad (8)$$

Let the error patterns in words be expressed as the sequence $(e_1, e_2, e_3, e_4, e_5, e_6, e_7, e_8)$ corresponding to the received word sequence, then

$$\begin{aligned} L'_{3n} &= L_{3n} \oplus e_1 \\ R'_{3n} &= R_{3n} \oplus e_2 \\ &\vdots \\ Q'_n &= Q_n \oplus e_8 \end{aligned} \quad (9)$$

Where, $\oplus$: Exclusive OR. (Modulo 2 addition)

From the equations (8) and (9), $S_1=S_2=0$ for no errors (i, e, $e_1=e_2=\ \ldots\ldots\ =e_8=0$).

From the equation (9) we obtain,

$$L_{3n} = L'_{3n} \oplus e_1$$

$$R_{3n} = R'_{3n} \oplus e_2 \qquad (10)$$

$$\vdots$$

$$R_{3n+2} = R'_{3n+2} \oplus e_6$$

This shows, the recovery of the words without errors is achieved by the addition in modulo 2 of the received data and error patterns. Note that, the check words are not needed to be recovered, and excluded in the equation (10).
The error patterns are obtained as follows,

3-2-1 In case of single error

(To be decoded by both parity decoding and b-Adjacent decoding.)
Assume the ith word is in error, then,

For $1 \leq i \leq 6$,

$$S_1 = e_i$$

$$S_2 = T^{7-i} e_i$$

The error pattern e_i is solved as,

$$e_i = S_1 \qquad \text{(error)} \qquad (11)$$

$$T^{i-7} S_2 = S_1 \qquad \text{(location)} \qquad (12)$$

The equation (11) gives the error pattern.

In case of parity decoding, the error pointer is used to locate the ith word being in error. While, in case of b-Adjacent decoding, the error location i is calculated from the equation (12). The advantage of this is to be able to prevent the misdetection of CRC.

3-2-2 In case of double errors

(To be decoded by b-Adjacent decoding, while the last case by parity decoding. The error locations are indicated by error pointers.)
Assume the ith and jth words are in error ($i < j$), then,

For $1 \leq i < j \leq 6$,

$$S_1 = e_i \oplus e_j$$

$$S_2 = T^{7-i} e_i \oplus T^{7-j} e_j$$

These equations can be solved for e_i and e_j to obtain,

$$e_j = (I \oplus T^{i-j})^{-1} (S_1 \oplus T^{i-7} S_2) \quad (13)$$

$$e_i = S_1 \oplus e_j = S_1 \oplus (I \oplus T^{i-j})^{-1} (S_1 \oplus T^{i-7} S_2) \quad (14)$$

For $1 \leq i \leq 6$, $j=7$

$$S_1 = e_i \oplus e_7$$

$$S_2 = T^{7-i} e_i$$

The error pattern e_i is obtained as,

$$e_i = T^{i-7} S_2 \quad (15)$$

For $1 \leq i \leq 6$, $j=8$

$$S_1 = e_i$$

$$S_2 = T^{7-i} e_i \oplus e_8$$

The error pattern e_i is obtained as,

$$e_i = S_1 \quad (16)$$

3-2-3 The Error Correction Capability

The interleaving gives 16H interval between each word as illustrated in Fig. 5. The parity decoding is effective when the error is not more than one. Accordingly, the burst error as long as 16H can be fully corrected. The probability that the parity decoding can not correct random errors is calculated as $P_H \cdot {}_6C_1 P_H = 6P^2_H$, where P_H is the error rate in the unit of H. As for the b-Adjacent decoding, like wise the burst error under 32H can be fully corrected and non-decodable probability for random errors is $P_H \cdot {}_7C_2 P_H{}^2 = 21P^3_H$. These are shown in Table 2.

4. Hardware Considerations

4-1 Encoder

Fig. 8 shows the schematic diagram of encoder. The check words are generated after accepting each block consisting of 6 data words as illustrated. The 14 bit shift register and Exclusive-OR compute the check word P by summing all the 6 data words in modulo 2. After the register is cleared, the first word L_{3n} is read into the register. when the second word R_{3n} is read into it, the register holds $L_{3n} \oplus R_{3n}$. This operation is repeated by 6 times. Then the final content in the register is,

$$L_{3n} \oplus R_{3n} \oplus L_{3n+1} \oplus R_{3n+1} \oplus L_{3n+2} \oplus R_{3n+2}$$

This is how the check word P_n is computed. Next, the 8 bit and 6 bit shift registers with feed back loop in the Fig. 8 serve as T operator. When the data d in them gets shifted by one bit with the gate G open, the result will be Td. Thus after the registers are cleard, the word L_{3n} is read into them with G closed and shifted by one bit with G open, then TL_{3n} is resulted. Followingly the word R_{3n} is read with G closed. At this time, TL_{3n} is added to R_{3n}. Accordingly, $R_{3n} \oplus TL_{3n}$ will remain in the registers. This is again shifted by one bit with G open. This shift operation is repeated by 6 times. Then, the result is,

$$T^6L_{3n} \oplus T^5R_{3n} \oplus T^4L_{3n+1} \oplus T^3R_{3n+1} \oplus T^2L_{3n+2} \oplus TR_{3n+2}$$

Thus, the check word Q_n is generated.

4-2 Decoder

Fig. 9 shows the schematic diagram of the decoder. The operation of the shift registers is the same as that in the encoder. The syndrome S_1 is computed by summing the received 6 data words plus the check word P'. The registers relating to the syndrome S_2 receive the 6 data words plus the check word Q', and so, the one bit shift for T operation is repeated by 7 times. Prior to the registers, T^{-8} is inserted. Thus, the result is $T^{-7}S_2$. Further, the i times shift is operated in accordance with the error location indicated by error pointers. Then we obtain $T^{i-7}S_2$. Furthermore, S_1 and $T^{i-7}S_2$ are added to be $S_1 \oplus T^{i-7}S_2$, and multiplied by $(I \oplus T^{i-j})^{-1}$ which is stored in the ROM.

Since both i and j are integers below 6, j-i varies from 1 to 5 holding $j > i$. It follows that the patterns of $(I \oplus T^{i-j})^{-1}$ come in five diffrent 14x14 bit matrices. The error patterns thus obtained are properly selected and added to the words in error in accordance with the error pointers.

We must consider the case that the received words may be in error but no pointers available because of the misdetection of CRC. To avoid this, (though the probability is low enough: $P_H \cdot 2^{-16}$) the schemes to detect $S_1=S_2=0$ may be implemented. Table 3 shows the mode of correction. When the parity decoding only is desired the circuitry relating to S_2 is excluded.

4-3 Memory Configuration

The PCM signal must be companded in time base in order to be transmitted using the TV signal format. Because as noted earlier, the 35 lines out of 525 lines in a frame shoud be excluded from data transmission. The ratio of companding is 14:15. Accordingly, the memory should be provided to store the data of 17 or 18 lines per field. In addition to this, the memory is needed for interleaving as well as de-interleaving and also for jitter absorption (required for the playback memory).

These memory schemes are realized by use of RAM's. Fig. 10 shows an example of the memory configuration for encoder. The RAM's consist of 20K; accounting for four 4x1K plus four 4x256. The data is processed in bit parallel.

The 3 bits are assigned to address the 6 data words and 2 check words. The 4 bits are assigned to address the 16 lines in each interleaving block. The 3 bits are for addressing the interleaving blocks. The 1 bit is for RAM select. In this configuration, we obtain 10 interleaving blocks consisting of 16 lines each, out of which 7 blocks are used for interleaving, 1 block plus 1 or 2 lines for time base compression, and the rest, about 2 blocks, is a margin. The words are written into horizontally and read out from the RAM's according to the number, along the line (1) so that the words get interleaved.

In designing the memory for decoder, the jitter absorption should be taken into consideration. For this, some additional 16-line-blocks may be required. Note that in the decoder, the words are read along the line (2). Fig. 11 shows the time chart of the memory.

5. Error Rate Measurements

With the use of the developed PCM audio processor being connected to VTR's, the following error rates have been measured.

5-1 Burst Run Length Distribution

The burst error signal is obtained from either the d.o.c out-put in the VTR or the CRC in the processor. Fig. 12 shows the measurements. The measurements with replacement of VTR's and tapes, showed the similar results. From the measurement, the maximum burst length is about as long as 4H detected by the d.o.c while 6H by CRC. This difference may presumably be coming from that the burst will take place in a group of comparatively short size of dropouts, and be detected continuous by the CRC. It is clear that the 16H interleaving is well effective.

Fig. 13 shows the difference between, (a) the tape is playback with the same VTR used for recording, and (b) with a different VTR. The difference is only slight. This means the interchangeability is secured.

5-2 Measurements of P_H and Concealed Word Rates

Non-decodable words are concealed by adequate interpolation. The mean value out of the ten different tapes, 5 minute measurement each, is shown in Table 4.

6. The Performance of the Processor

The specifications of the Processors D-1 and, D-1L are as follows.

Modulation	PCM using NTSC TV format
Channels	2cH
Frequency Response	DC – 20 kHz ($\pm$0.5 dB)
Dynamic Range	Better than 90dB with Emphasis ON
Emphasis	ON-OFF switchable
T.H.D.	D-1 : 0.03 % D-1L: 0.02 %
Sampling Frequency	44.056 kHz
Transmission Rate	2.643 Mbps
Quantization (Both Encoder and Decoder)	D-1 : 3 segment 12 bit companding D-1L: 14 bit linear
Wow and Flutter	Undetectable
Dropout Compensation	Correction by interleaved b-Adjacent error correction code with CRC
Signal Format	Based on the EIAJ Technical File STC-007
Conforming VTR's	VHS, β , U etc.

The schematic block diagram of the Processor is shown in Fig. 14. Fig. 15 shows the Total Harmonic Distortions vs. Input Level. Fig. 16 shows the Frequency Response. Fig. 17 shows the eye diagram of the reproduced signal from a VTR. In the upper right, the wave of White Reference is seen. Note that the White Reference is inserted to insure the wave transmission through VTR's where the AGC is implemented. Fig. 18 shows the external view of the processor.

7. Comments on PAL/SECAM Version (2)

The PAL/SECAM employs 625 lines, 50 fields. The basic parameters such as sampling frequency and transmission rate will be chosen like in section 2-2. The basic relationship corresponding to the equation (1) is,

$$F_S = M \cdot F_h \cdot \frac{625-x}{625}$$
$$= M \cdot F_h \cdot \frac{n}{m} \qquad (16)$$

Where F_h = 15.625 kHz

Table 5 shows some possible examples of M, x, m, n, and F_S for PAL/SECAM version. The sampling frequency is desired to be common to both NTSC and PAL/SECAM. However this will not be possible because of the inherent difference between the two television systems. The second best is to keep the difference minimum. Then we obtain from the Table 5,

$$M = 3, \quad x = 37, \quad F_S = 44.1 \text{ kHz}$$
$$n/m \simeq 588/625$$

The difference between two F_S's is 0.1 %. The total bits per line N will be desired to be chosen 168 equal to that in NTSC, then,

$$F_C = N \cdot F_h$$
$$= 2.625 \text{ Mbps}$$

Fig. 19 shows the inter-relations of clocks for PAL/SECAM.

8. Conclusion

The authors described the outline of the standardized format for a PCM audio processor as well as the system designing. Since the signal format is conforming to NTSC, the system is desired to be used for many applications, such as broadcasting of audio PCM over television networks, etc.

9. Acknowledgement

The authors express their appreciation to Mr. M. Ishida and Mr. S. Shibuya for their cooperations in designing the processor.

10. References

(1) EIAJ Technical File STC-007.

(2) K. Tanaka and Y. Ishida. "Sampling Frequency Consideration." Journal of AES. (1978-4)

(3) Y. Ishida et al. "A ROTARY-HEAD PCM RECORDER EMPLOYING ERROR CORRCTION TECHNIQUE." IE^3 Vol. CE-24 No.4 (1978-11)

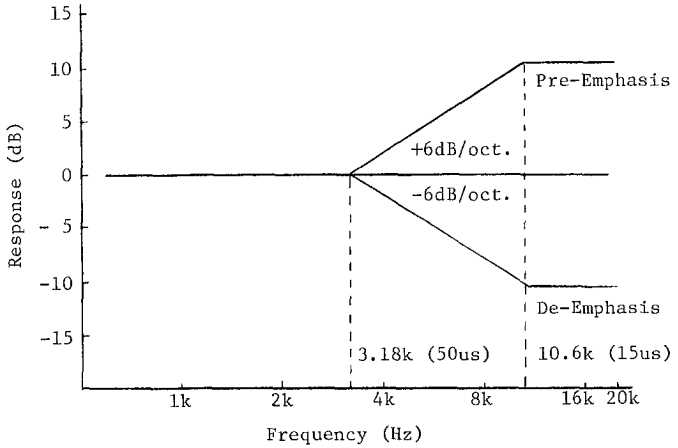


Fig. 1 Emphasis.

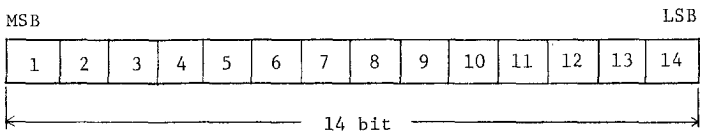
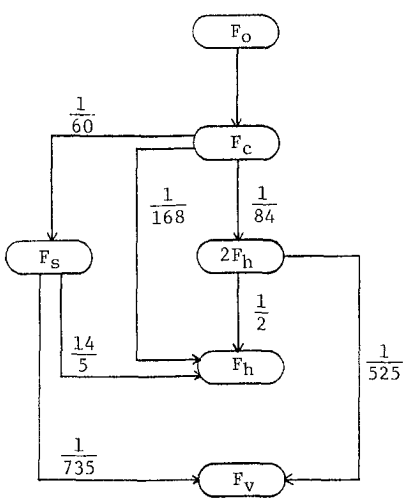


Fig. 2 14 bit Slot.



Note

F_o Master Clock

F_c Transmission Rate

F_h Horizontal Rate

F_s Sampling Rate

F_v Vertical Rate

Fig. 3 Relations of Clocks. (NTSC)

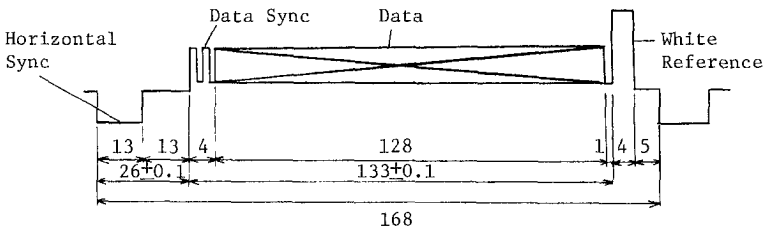


Fig. 4 1H Format. (unit: in bits)

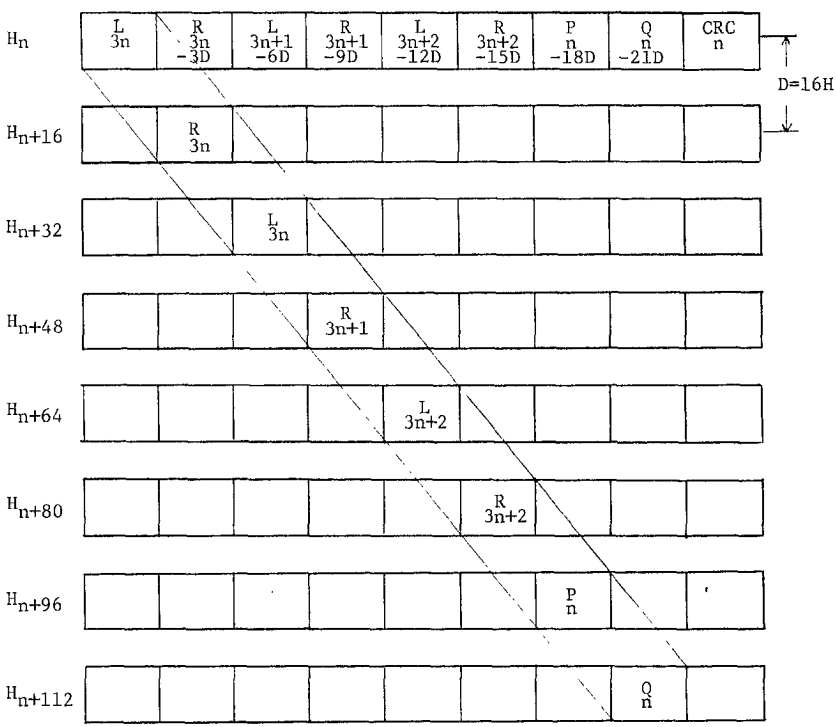


Fig. 5 Interleaving.

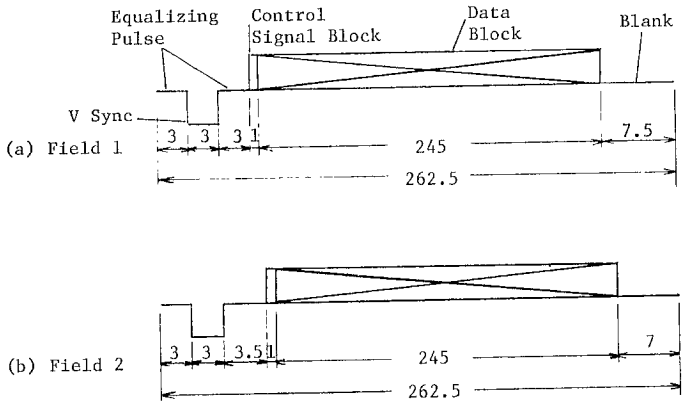


Fig. 6 1 Field Format. (unit: in H)

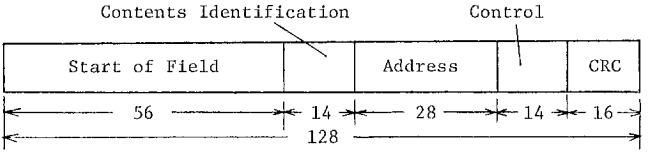
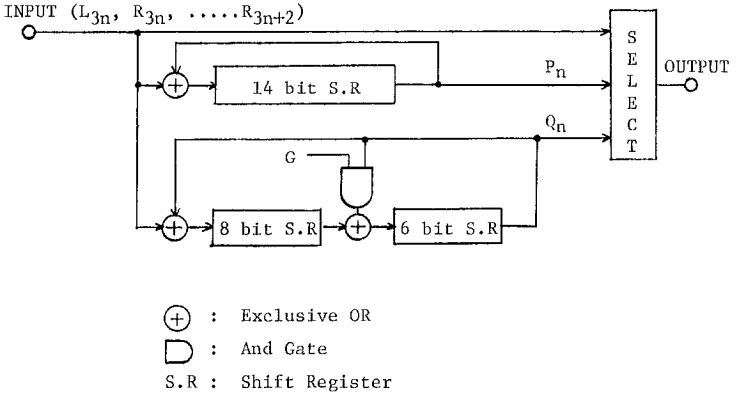


Fig. 7 Control Signal Block. (unit: in bits)



⊕ : Exclusive OR

D : And Gate

S.R : Shift Register

Fig. 8 Encoder.

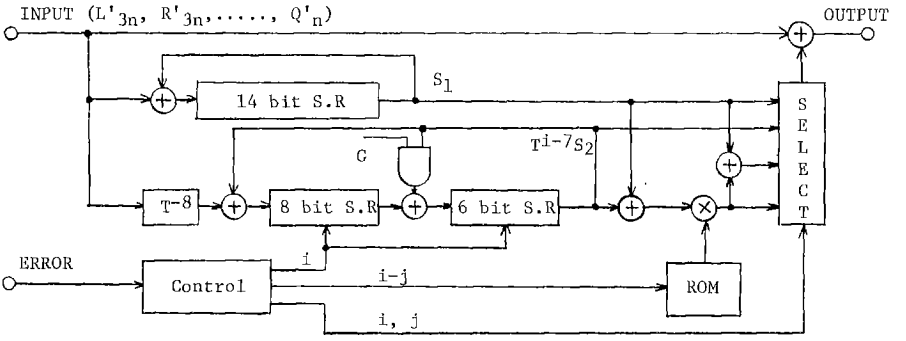


Fig. 9 Decoder.

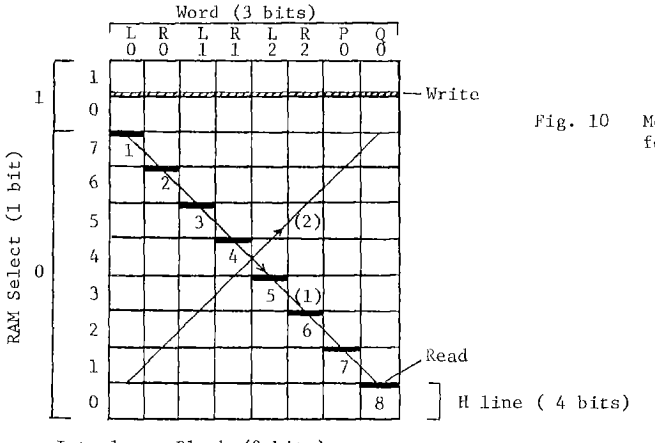
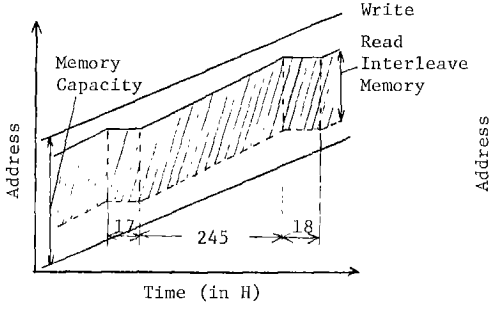
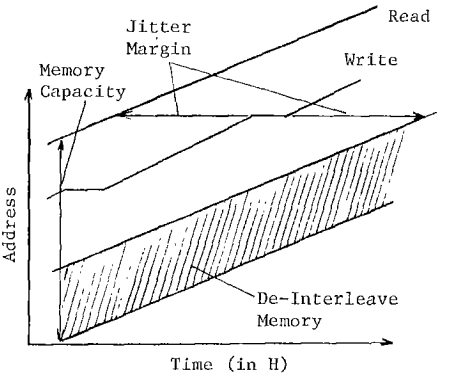


Fig. 10 Memory Configuration for Encoder

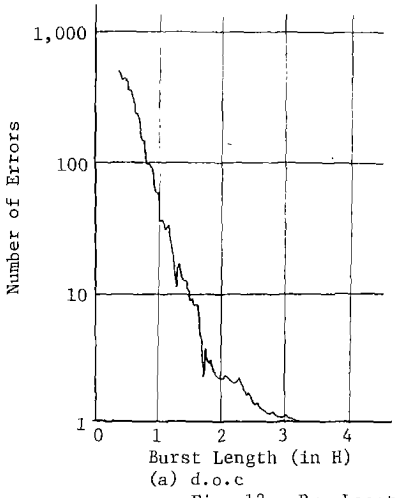


(a) Encoder

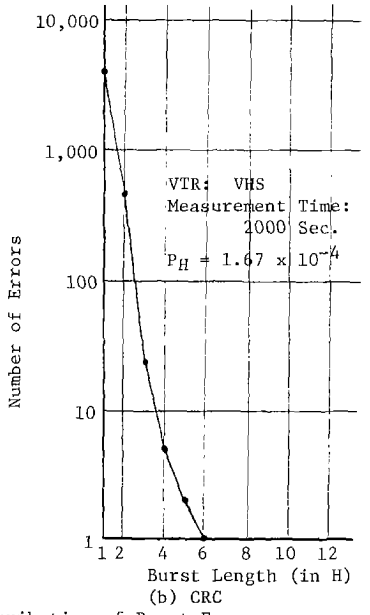


(b) Decoder

Fig. 11 Time Chart of Memories.

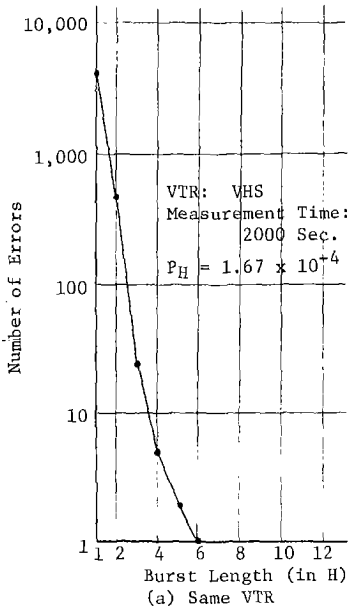


(a) d.o.c

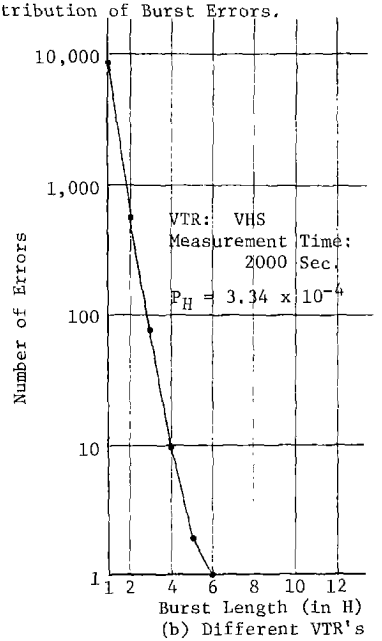


(b) CRC

Fig. 12 Run Length Distribution of Burst Errors.



(a) Same VTR



(b) Different VTR's

Fig. 13 Interchangeability

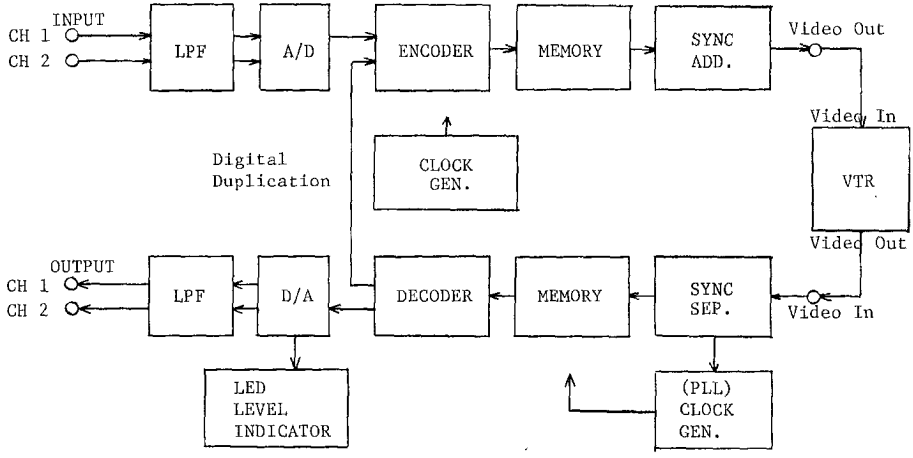


Fig. 14 Schematic Block Diagram.

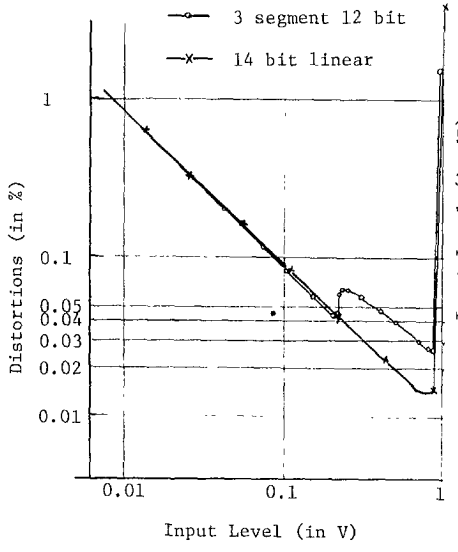


Fig. 15 T.H.D vs. Level.

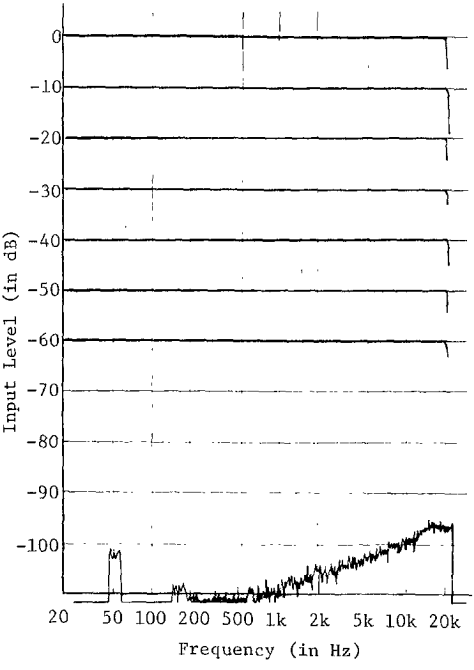


Fig. 16 Frequency Response.

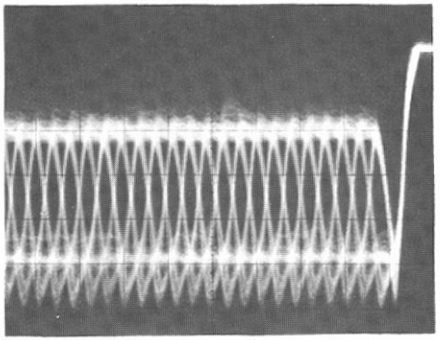


Fig. 17 Eye Diagram.

Fig. 18 External View.

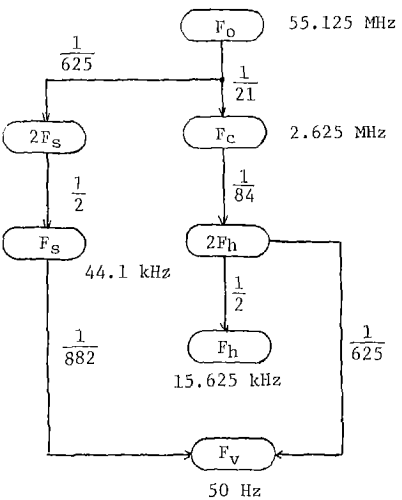


Fig. 19 Interrelations of Clocks. (PAL/SECAM)

Table 1 Relations of M, x, n, m, F_S of NTSC

M	x	n	m	F_S (kHz)
3	32	493	525	44.326
	33	164	175	44.236
	34	491	525	44.146
	35	14	15	44.056
	36	163	175	43.966
	37	488	525	43.876
	38	487	525	43.786
4	32	493	525	59.101
	33	164	175	58.981

Table 5 Relation of M, x, n, m, F_S of PAL/SECAM

M	x	n	m	F_S (kHz)
3	34	591	625	44.325
	35	118	125	44.250
	36	589	625	44.175
	37	588	625	44.100
	38	587	625	44.025
	39	586	625	43.950
	40	117	125	43.875
4	34	591	625	59.100
	35	118	125	59.000

Table 2 Error Correction capability

Error \ Decoder	Parity	b-Adjacent
RANDOM Concealment Prob.	$6P^2_H$	$21P^3_H$
BURST Correction	0 - 16H	0 - 32H
Concealment	16 - 32H	32 - 64H

PH: H error rate

Table 3 Mode of Correction

Total Errors	in 6 Data Words	in P	in Q	Correction Mode
0	0	0	0	Pass
1	1	0	0	P corr.
	0	1	0	Pass
	0	0	1	Pass
2	2	0	0	P Q corr.
	1	1	0	Q corr.
	1	0	1	P corr.
	0	1	1	Pass
≥3				Conceal

Table 4 Concealed Word Rate

H Error Rate	P_H	1.17×10^{-4}
Concealed Word Rate	Parity	3.91×10^{-7}
	b-Adjacent	0

Mean Value of 10 measurments